

PIC16F/LF1825/1829 Data Sheet

14/20-Pin Flash Microcontrollers with nanoWatt XLP Technology

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ISBN: 978-1-60932-473-5

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14/20-Pin Flash Microcontrollers with nanoWatt Technology

High-Performance RISC CPU:

- Only 49 Instructions to Learn:
 - All single-cycle instructions except branches
- Operating Speed:
 - DC 32 MHz oscillator/clock input
 - DC 125 ns instruction cycle
- Up to 8 Kbytes Linear Program Memory Addressing
- Up to 1024 bytes Linear Data Memory Addressing
- · Interrupt Capability with automatic context saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
 - Two full 16-bit File Select Registers (FSRs)
 - FSRs can read program and data memory

Flexible Oscillator Structure:

- Precision 32 MHz Internal Oscillator Block:
- Factory calibrated to ± 1%, typical
- Software selectable frequencies range of 31 kHz to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- · Four Crystal modes up to 32 MHz
- · Three External Clock modes up to 32 MHz
- 4X Phase Lock Loop (PLL)
- Fail-Safe Clock Monitor:
- Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up
- Reference Clock Module:
 - Programmable clock output frequency and duty-cycle

Special Microcontroller Features:

- 1.8V-5.5V Operation PIC16F1825/1829
- 1.8V-3.6V Operation PIC16LF1825/1829
- Self-Programmable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Brown-out Reset (BOR)
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™) via two pins
- · In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Operating Voltage Range:
 - 1.8V-5.5V (PIC16F1825/1829)
 - 1.8V-3.6V (PIC16LF1825/1829)
- Programmable Code Protection
- Power-Saving Sleep mode

Extreme Low-Power Management PIC16LF1825/1829 with nanoWatt XLP:

- Sleep mode: 20 nA
- Watchdog Timer: 500 nA
- Timer1 Oscillator: 600 nA @ 32 kHz

Analog Features:

- Analog-to-Digital Converter (ADC) Module:
 - 10-bit resolution, up to 12 channels
 - Auto acquisition capability
 - Conversion available during Sleep
- Analog Comparator Module:
 - Two rail-to-rail analog comparators
 - Power mode control
- Software controllable hysteresis
- Voltage Reference Module:
 - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
 - 5-bit rail-to-rail resistive DAC with positive and negative reference selection

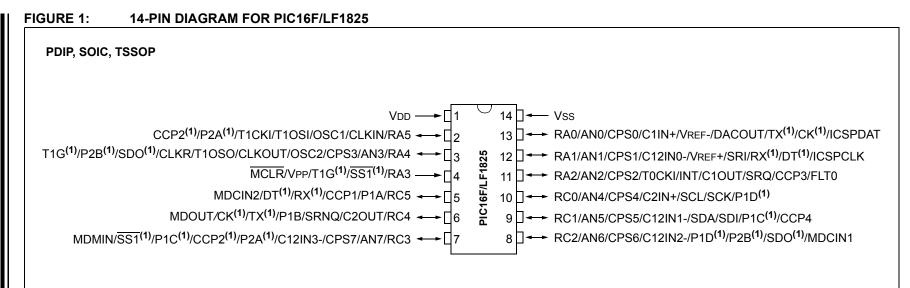
Peripheral Highlights:

- Up to 17 I/O Pins and 1 Input Only Pin:
- High current sink/source 25 mA/25 mA
 - Programmable weak pull-ups
- Programmable interrupt-on-change pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Gate Input mode
 - Dedicated, low-power 32 kHz oscillator driver
- Three Timer2-types: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture, Compare, PWM (CCP) Modules
- Two Enhanced CCP (ECCP) Modules:
- Software selectable time bases
- Auto-shutdown and auto-restart
- PWM steering
- Up to two Master Synchronous Serial Port (MSSP) with SPI and I²C[™] with:
 - 7-bit address masking
 - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) Module
- mTouch[™] Sensing Oscillator Module:
- Up to 12 input channelsData Signal Modulator Module:
- Selectable modulator and carrier sources
- SR Latch:
 - Multiple Set/Reset input options
 - Emulates 555 Timer applications

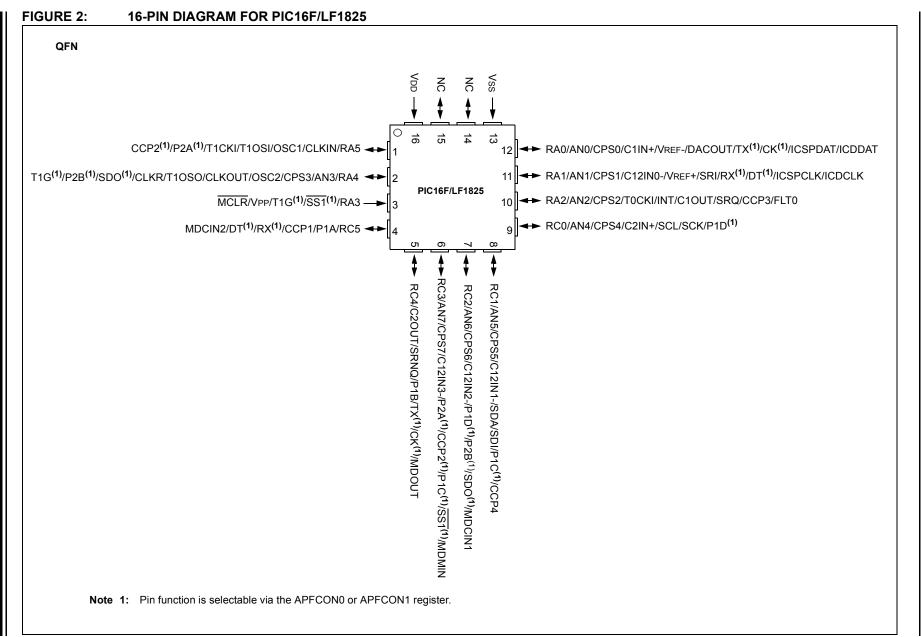
PIC16F/LF1825/1829 Family Types

	Program Memory	-	ata nory		(ch)	(ch)	S	-bit)			tridge)	idge)		
Device	Words	SRAM (bytes)	Data EEPROM (bytes)	I/O's ⁽¹⁾	10-bit ADC (Cap Sense (Comparato	Timers (8/16	EUSART	dSSM	ECCP (Full-Br	ECCP (Half-Bridge)	CCP	SR Latch
PIC16LF1825	8K	1024	256	12	8	8	2	4/1	1	1	1	1	2	Yes
PIC16F1825	8K	1024	256	12	8	8	2	4/1	1	1	1	1	2	Yes
PIC16LF1829	8K	1024	256	18	12	12	2	4/1	1	2	1	1	2	Yes
PIC16F1829	8K	1024	256	18	12	12	2	4/1	1	2	1	1	2	Yes

Note 1: One pin is input only.



Note 1: Pin function is selectable via the APFCON0 or APFCON1 register.

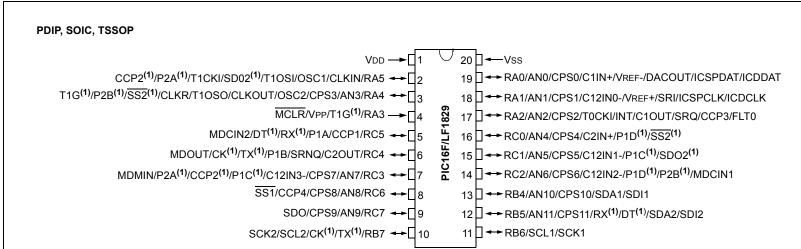


IABL			14-6		10-F	IN ALLU	CAIL			JIOF/L	г 1025)	-	-		
0/1	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	ECCP	EUSART	ASSM	Interrupt	Modulator	Pull-up	Basic
RA0	13	12	AN0	VREF- DACOUT	CPS0	C1IN+			_	TX ⁽¹⁾ CK ⁽¹⁾		IOC	_	Y	ICSPDAT ICDDAT
RA1	12	11	AN1	VREF+	CPS1	C12IN0-	SRI			RX ⁽¹⁾ DT ⁽¹⁾		IOC	_	Y	ICSPCLK ICDCLK
RA2	11	10	AN2	_	CPS2	C10UT	SRQ	TOCKI	CCP3 FLT0			INT/ IOC	_	Y	—
RA3	4	3	—	_	—	_	_	T1G ⁽¹⁾	_	_	SS1 ⁽¹⁾	IOC	_	Y	MCLR VPP
RA4	3	2	AN3	_	CPS3	_	_	T1G ⁽¹⁾ T1OSO	P2B ⁽¹⁾	_	SDO ⁽¹⁾	IOC	_	Y	OSC2 CLKOUT CLKR
RA5	2	1	_	—			—	T1CKI T1OSI	CCP2 P2A ⁽¹⁾			IOC	—	Y	OSC1 CLKIN
RC0	10	9	AN4		CPS4	C2IN+			P1D ⁽¹⁾		SCL SCK		_	Y	—
RC1	9	8	AN5	_	CPS5	C12IN1-	_		CCP4 P1C ⁽¹⁾		SDA SDI		_	Y	—
RC2	8	7	AN6		CPS6	C12IN2-			P1D ⁽¹⁾ P2B ⁽¹⁾		SDO ⁽¹⁾		MDCIN1	Y	—
RC3	7	6	AN7	_	CPS7	C12IN3-			CCP2 ⁽¹⁾ P1C ⁽¹⁾ P2A ⁽¹⁾		SS1 ⁽¹⁾		MDMIN	Y	—
RC4	6	5	—	_	-	C2OUT	SRNQ		P1B	TX ⁽¹⁾ CK ⁽¹⁾			MDOUT	Y	_
RC5	5	4	—	_			_		CCP1 P1A	RX ⁽¹⁾ DT ⁽¹⁾			MDCIN2	Y	—
Vdd	1	16	—	—	—	_	—	—	—	—	_	—	—	—	Vdd
Vss	14	13	—	—	—	—	—	—	—	—	_	—	—	—	Vss

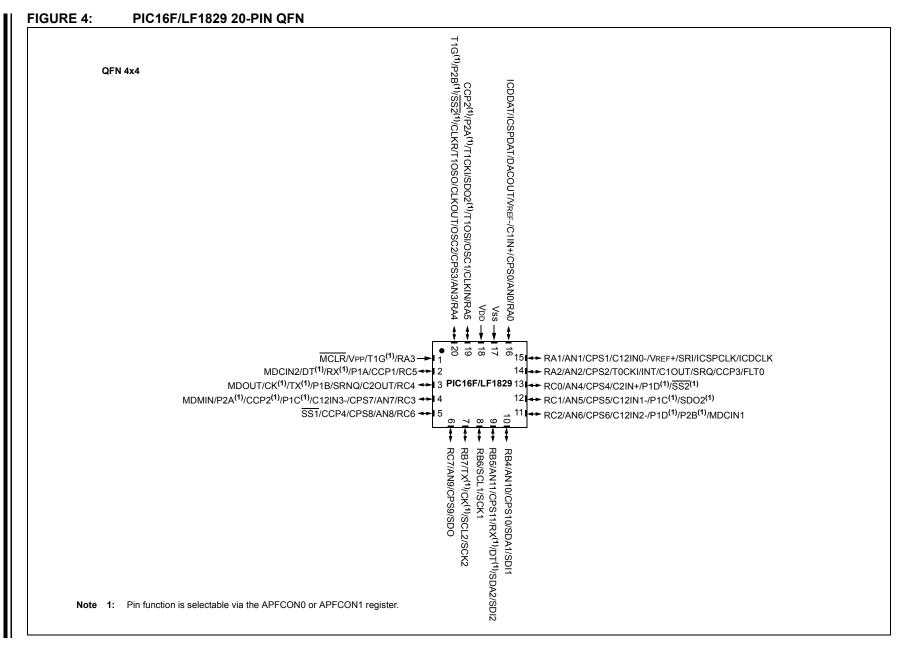
TABLE 1: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16F/LF1825)

Note 1: Pin function is selectable via the APFCON0 or APFCON1 register.

FIGURE 3: 20-PIN DIAGRAM FOR PIC16F/LF1829



Note 1: Pin function is selectable via the APFCON0 or APFCON1 register.



IADLE			201	IN ALLC					11020)		-				
Q	20-Pin PDIP/SOIC/TSSOP	20-Pin QFN	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	ССР	EUSART	SSP	Interrupt	Modulator	Pull-up	Basic
RA0	19	16	AN0	VREF- DACOUT	CPS0	C1IN+	_	_	_	—	_	IOC	-	Y	ICSPDAT/ ICDDAT
RA1	18	15	AN1	VREF+	CPS1	C12IN0-	SRI	—	_	—	_	IOC	—	Y	ICSPCLK/ ICDCLK
RA2	17	14	AN2	—	CPS2	C1OUT	SRQ	TOCKI	CCP3 FLT0	—	-	INT/ IOC		Y	-
RA3	4	1		—				T1G ⁽¹⁾		—		IOC	—	Y ⁽⁴⁾	MCLR VPP
RA4	3	20	AN3	_	CPS3			T1G ⁽¹⁾ T1OSO	P2B ⁽¹⁾	_	SS2 ⁽¹⁾	IOC	-	Y	OSC2 CLKOUT CLKR
RA5	2	19	_	—	_	_	-	T1CKI T1OSI	CCP2 ⁽¹⁾ P2A ⁽¹⁾	—	SDO2 ⁽¹⁾	IOC	—	Y	OSC1 CLKIN
RB4	13	10	AN10	—	CPS10	—		—	_	—	SDA1 SDI1	IOC	-	Y	-
RB5	12	9	AN11	—	CPS11	_	_	—	_	RX ⁽¹⁾ DT ⁽¹⁾	SDA2 SDI2	IOC	-	Y	—
RB6	11	8	_	—	-	_	-	_	_	—	SCL1 SCK1	IOC	-	Y	-
RB7	10	7	_	—	_	_	—	—	_	TX ⁽¹⁾ CK ⁽¹⁾	SCL2 SCK2	IOC	—	Y	—
RC0	16	13	AN4	—	CPS4	C2IN+	—	—	P1D ⁽¹⁾	—	SS2 ⁽¹⁾		—	Y	—
RC1	15	12	AN5	_	CPS5	C12IN1-	_	_	P1C ⁽¹⁾	—	SDO2 ⁽¹⁾	_	—	Y	—
RC2	14	11	AN6	—	CPS6	C12IN2-		_	P1D ⁽¹⁾ P2B ⁽¹⁾	—	-	—	MDCIN1	Y	—
RC3	7	4	AN7	_	CPS7	C12IN3-		Ι	P1C ⁽¹⁾ CCP2 ⁽¹⁾ P2A ⁽¹⁾	_	_	_	MDMIN	Y	_
RC4	6	3	_	—	-	C2OUT	SRNQ		P1B	TX ⁽¹⁾ CK ⁽¹⁾	-	—	MDOUT	Y	-
RC5	5	2		—		-	—	—	CCP1 P1A	RX ⁽¹⁾ DT ⁽¹⁾	_	—	MDCIN2	Y	—
RC6	8	5	AN8	—	CPS8		—	_	CCP4	—	SS1	_	—	Y	—
RC7	9	6	AN9	_	CPS9	_	—	_	_	_	SDO	_	_	Y	_
Vdd	1	18	—	—	—		—	_	_	—	_	_	—	—	Vdd
Vss	20	17	_	_	—	—	—	_	_	—	—	_	—	_	Vss
Note 1	•	Pin f	unction i	s selectable	via the A	PECONO		N1 register							

TABLE 2: 20-PIN ALLOCATION TABLE (PIC16F/LF1829)

Note 1: Pin function is selectable via the APFCON0 or APFCON1 register.

Table of Contents

1.0 Device Overview	13
2.0 Enhanced Mid-range CPU	21
3.0 Memory Organization	23
4.0 Device Configuration	
5.0 Oscillator Module (With Fail-Safe Clock Monitor)	
6.0 Reference Clock Module	
7.0 Resets	
8.0 Interrupts	
9.0Power-Down Mode (Sleep)	103
10.0Watchdog Timer	
11.0Data EEPROM and Flash Program Memory Control	109
12.0 I/O Ports	123
13.0 Interrupt-On-Change	
14.0 Fixed Voltage Reference (FVR)	147
15.0 Temperature Indicator Module	149
16.0 Analog-to-Digital Converter (ADC) Module	151
17.0 Digital-to-Analog Converter (DAC) Module	
18.0 SR Latch	171
19.0 Comparator Module	177
20.0 Timer0 Module	
21.0 Timer1 Module with Gate Control	191
22.0 Timer2/4/6 Modules	203
23.0 Data Signal Modulator	
24.0 Capture/Compare/PWM Modules	
25.0 Master Synchronous Serial Port (MSSP1 and MSSP2) Module	
26.0 Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	
27.0 Capacitive Sensing (CPS) Module	
28.0 In-Circuit Serial Programming™ (ICSP™)	
29.0 Instruction Set Summary	339
30.0 Electrical Specifications	
31.0 DC and AC Characteristics Graphs and Charts	
32.0 Development Support	
33.0 Packaging Information	
Appendix A: Data Sheet Revision History	
Appendix B: Migrating From Other PIC® Devices	409
The Microchip Web Site	
Customer Change Notification Service	
Customer Support	
Reader Response	
Product Identification System	421
Worldwide Sales and Service	

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1.0 DEVICE OVERVIEW

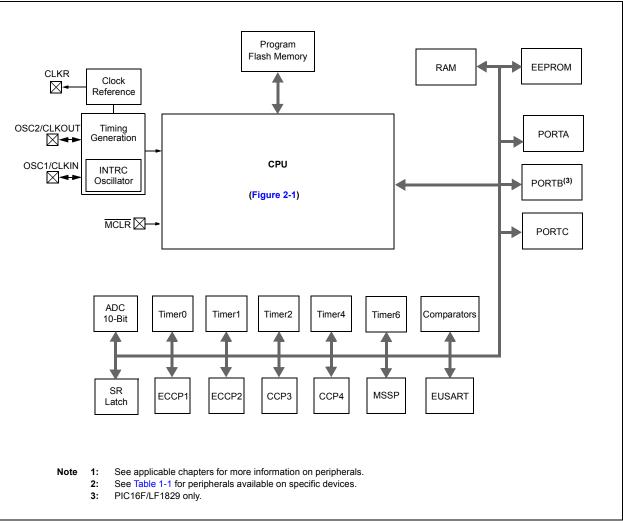
The PIC16F/LF1825/1829 are described within this data sheet. They are available in 14/20 pin packages. Figure 1-1 shows a block diagram of the PIC16F/LF1825/1829 devices. Tables 1-2 and 1-3 show the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1:DEVICE PERIPHERALSUMMARY

Peripheral		PIC16F/LF1825	PIC16F/LF1829
ADC		•	•
Capacitive Sensing (CF	•	•	
Data EEPROM	•	•	
Digital-to-Analog Conve	•	•	
Digital Signal Modulator	•	•	
EUSART		•	•
Fixed Voltage Referenc	e (FVR)	•	•
SR Latch		٠	•
Capture/Compare/PWN	1 Modules		
	ECCP1	٠	•
	ECCP2	٠	•
	CCP3	•	•
	CCP4	•	•
Comparators			
	C1	•	•
	C2	•	•
Master Synchronous Se	erial Ports		
	MSSP1	•	•
	MSSP2		•
Timers			
	Timer0	•	•
	Timer1	•	•
	Timer2	•	•
	Timer4	•	•
	Timer6	•	•





	102311110		-	
Name	Function	Input Type	Output Type	Description
RA0/AN0/CPS0/C1IN+/VREF-/	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN		A/D Channel 0 input.
ICSPDAT/ICDDAT	CPS0	AN		Capacitive sensing input 0.
	C1IN+	AN		Comparator C1 positive input.
	VREF-	AN	—	A/D and DAC Negative Voltage Reference input.
	DACOUT	_	AN	Digital-to-Analog Converter output.
	TX	_	CMOS	USART asynchronous transmit.
	СК	ST	CMOS	USART synchronous clock.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
RA1/AN1/CPS1/C12IN0-/VREF+/	RA1	TTL	CMOS	General purpose I/O.
SRI/RX ⁽¹⁾ /DT ⁽¹⁾ /ICSPCLK/	AN1	AN	_	A/D Channel 1 input.
ICDCLK	CPS1	AN		Capacitive sensing input 1.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	VREF+	AN	_	A/D and DAC Positive Voltage Reference input.
	SRI	ST	_	SR Latch input.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	ICSPCLK	ST	_	Serial Programming Clock.
	ICDCLK	ST	_	In-Circuit Debug Clock.
RA2/AN2/CPS2/T0CKI/INT/	RA2	ST	CMOS	General purpose I/O.
C1OUT/SRQ/CCP3/FLT0	AN2	AN	_	A/D Channel 2 input.
	CPS2	AN	—	Capacitive sensing input 2.
	TOCKI	ST	_	Timer0 clock input.
	INT	ST	_	External interrupt.
	C10UT		CMOS	Comparator C1 output.
	SRQ		CMOS	SR Latch non-inverting output.
	CCP3	ST	CMOS	Capture/Compare/PWM 3.
	FLT0	ST	_	ECCP Auto-Shutdown Fault input.
RA3/SS1 ⁽¹⁾ /T1G ⁽¹⁾ /VPP/MCLR	RA3	TTL	—	General purpose input.
	SS1	ST	—	Slave Select input.
	T1G	ST	—	Timer1 Gate input.
	VPP	ΗV	—	Programming voltage.
	MCLR	ST		Master Clear with internal pull-up.

TABLE 1-2: PIC16F/LF1825 PINOUT DESCRIPTION

Legend:AN = Analog input or outputCMOS = CMOS compatible input or outputOD= Open DrainTTL = TTL compatible inputST= Schmitt Trigger input with CMOS levels I^2C^{TM} = Schmitt Trigger input with I^2C HV = High VoltageXTAL= Crystallevels

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.

TABLE 1-2: PIC16F/LF1825 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA4/AN3/CPS3/OSC2/	RA4	TTL	CMOS	General purpose I/O.
CLKOUT/T1OSO/CLKR/ SDO ⁽¹⁾ /P2B ⁽¹⁾ /T1G ^(1,2)	AN3	AN		A/D Channel 3 input.
SDO("/P2B("/11G("-	CPS3	AN	_	Capacitive sensing input 3.
	OSC2		CMOS	Comparator C2 output.
	CLKOUT	_	CMOS	Fosc/4 output.
	T10SO	XTAL	XTAL	Timer1 oscillator connection.
	CLKR	—	CMOS	Clock Reference output.
	SDO	—	CMOS	SPI data output.
	P2B	—	CMOS	PWM output.
	T1G	ST	_	Timer1 Gate input.
RA5/CLKIN/OSC1/T1OSI/	RA5	TTL	CMOS	General purpose I/O.
T1CKI/P2A ⁽¹⁾ /CCP2 ⁽¹⁾	CLKIN	CMOS	—	External clock input (EC mode).
	OSC1	XTAL	_	Crystal/Resonator (LP, XT, HS modes).
	T10SI	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	_	Timer1 clock input.
	P2A	—	CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM 2.
RC0/AN4/CPS4/C2IN+/SCL/	RC0	TTL	CMOS	General purpose I/O.
SCK/P1D ⁽¹⁾	AN4	AN	_	A/D Channel 4 input.
	CPS4	AN	_	Capacitive sensing input 4.
	C2IN+	AN	_	Comparator C2 positive input.
	SCL	l ² C	OD	I ² C™ clock.
	SCK	ST	CMOS	SPI clock.
	P1D	—	CMOS	PWM output.
RC1/AN5/CPS5/C12IN1-/SDA/	RC1	TTL	CMOS	General purpose I/O.
SDI/P1C ⁽¹⁾ /CCP4	AN5	AN	—	A/D Channel 5 input.
	CPS5	AN	_	Capacitive sensing input 5.
	C12IN1-	AN	_	Comparator C1 or C2 negative input.
	SDA	l ² C	OD	I ² C data input/output.
	SDI	CMOS		SPI data input.
	P1C	_	CMOS	PWM output.
	CCP4	AN		Capacitive sensing input 4.
RC2/AN6/CPS6/C12IN2-/	RC2	TTL	CMOS	General purpose I/O.
P1D ^(1,2) /P2B ^(1,2) /SDO ^(1,2) /	AN6	AN	—	A/D Channel 6 input.
MDCIN1	CPS6	AN		Capacitive sensing input 6.
	C12IN2-	AN		Comparator C1 or C2 negative input.
	P1D	—	CMOS	PWM output.
	P2B		CMOS	PWM output.
	SDO	—	CMOS	SPI data output.
	MDCIN1	ST	_	Modulator Carrier Input 1.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C^{TM} = Schmitt Trigger input with I^2C

levels

HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.

Name	Function	Input Type	Output Type	Description
RC3/AN7/CPS7/C12IN3-/	RC3	TTL	CMOS	General purpose I/O.
$P2A^{(1,2)}/CCP2^{(1,2)}/P1C^{(1,2)}/$	AN7	AN		A/D Channel 7 input.
SS1 ^(1,2) /MDMIN	CPS7	AN	_	Capacitive sensing input 7.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
	P2A	_	CMOS	PWM output.
	CCP2	AN	—	Capacitive sensing input 2.
	P1C	_	CMOS	PWM output.
	SS1	ST	_	Slave Select input.
	MDMIN	ST	_	Modulator source input.
RC4/C2OUT/SRNQ/P1B/TX ^(1,2) /	RC4	TTL	CMOS	General purpose I/O.
CK ^(1,2) /MDOUT	C2OUT		CMOS	Comparator C2 output.
	SRNQ		CMOS	SR Latch inverting output.
	P1B		CMOS	PWM output.
	ТХ		CMOS	USART asynchronous transmit.
	СК	ST	CMOS	USART synchronous clock.
	MDOUT		CMOS	Modulator output.
RC5/P1A/CCP1/DT ^(1,2) /RX ^(1,2) /	RC5	TTL	CMOS	General purpose I/O.
MDCIN2	P1A		CMOS	PWM output.
	CCP1	ST	CMOS	Capture/Compare/PWM 1.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	MDCIN2	ST	—	Modulator Carrier Input 2.
Vdd	Vdd	Power	—	Positive supply.
Vss	Vss	Power	_	Ground reference.

TABLE 1-2: PIC16F/LF1825 PINOUT DESCRIPTION (CONTINUED)

TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C^{TM} = Schmitt Trigger input with I^2C HV = High Voltage XTAL = Crystal levels

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.

TABLE 1-3: **PIC16F/LF1829 PINOUT DESCRIPTION**

Name	Function	Input Type	Output Type	Description
RA0/AN0/CPS0/C1IN+/VREF-/	RA0	TTL	CMOS	General purpose I/O.
DACOUT/ICSPDAT/ICDDAT	AN0	AN	_	A/D Channel 0 input.
	CPS0	AN		Capacitive sensing input 0.
	C1IN+	AN		Comparator C1 positive input.
	VREF-	AN	—	A/D and DAC Negative Voltage Reference input.
	DACOUT	_	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
RA1/AN1/CPS1/C12IN0-/VREF+/	RA1	TTL	CMOS	General purpose I/O.
SRI/ICSPCLK/ICDCLK	AN1	AN	_	A/D Channel 1 input.
	CPS1	AN	_	Capacitive sensing input 1.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	VREF+	AN	—	A/D and DAC Positive Voltage Reference input.
	SRI	ST	_	SR Latch input.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	_	In-Circuit Debug Clock.
RA2/AN2/CPS2/T0CKI/INT/	RA2	ST	CMOS	General purpose I/O.
C1OUT/SRQ/CCP3/FLT0	AN2	AN	_	A/D Channel 2 input.
	CPS2	AN	_	Capacitive sensing input 2.
	TOCKI	ST	_	Timer0 clock input.
	INT	ST	—	External interrupt.
	C10UT	_	CMOS	Comparator C1 output.
	SRQ		CMOS	SR Latch non-inverting output.
	CCP3	ST	CMOS	Capture/Compare/PWM 3.
	FLT0	ST	_	ECCP Auto-Shutdown Fault input.
RA3/T1G ⁽¹⁾ /VPP/MCLR	RA3	TTL	_	General purpose input.
	T1G	ST	—	Timer1 Gate input.
	VPP	ΗV	—	Programming voltage.
	MCLR	ST	_	Master Clear with internal pull-up.
RA4/AN3/CPS3/OSC2/	RA4	TTL	CMOS	General purpose I/O.
CLKOUT/T1OSO/CLKR/ <u>SS2⁽¹⁾/</u> P2B ⁽¹⁾ /T1G ^(1,2)	AN3	AN	—	A/D Channel 3 input.
P2B ⁽ⁱ⁾ /IIG ⁽ⁱ⁾	CPS3	AN	_	Capacitive sensing input 3.
	OSC2	_	CMOS	Comparator C2 output.
	CLKOUT	_	CMOS	Fosc/4 output.
	T10S0	XTAL	XTAL	Timer1 oscillator connection.
	CLKR	_	CMOS	Clock Reference output.
	SS2	ST	_	Slave Select input 2.
	P2B	_	CMOS	PWM output.
	T1G	ST		Timer1 Gate input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C^{TM} = Schmitt Trigger input with I^2C XTAL = Crystal ΗV

levels

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.

Name	Function	Input Type	Output Type	Description
RA5/CLKIN/OSC1/T1OSI/	RA5	TTL	CMOS	General purpose I/O.
SD02 ⁽¹⁾ /T1CKI/P2A ⁽¹⁾ /CCP2 ⁽¹⁾	CLKIN	CMOS	_	External clock input (EC mode).
	OSC1	XTAL	_	Crystal/Resonator (LP, XT, HS modes).
	T10SI	XTAL	XTAL	Timer1 oscillator connection.
	SD02		CMOS	SPI data output 2.
	T1CKI	ST		Timer1 clock input.
	P2A	—	CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM 2.
RB4/AN10/CPS10/SDA1/SDI1	RB4	TTL	CMOS	General purpose I/O.
	AN10	AN	_	A/D Channel 10 input.
	CPS10	AN	_	Capacitive sensing input 10.
	SDA1	l ² C	OD	I ² C™ data input/output.
	SDI1	CMOS	_	SPI data input.
RB5/AN11/CPS11/RX ^(1,2) /	RB5	TTL	CMOS	General purpose I/O.
DT ^(1,2) /SDA2/SDI2	AN11	AN	_	A/D Channel 11 input.
	CPS11	AN	_	Capacitive sensing input 11.
	RX	ST	_	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	SDA2	l ² C	OD	I ² C data input/output 2.
	SDI2	CMOS	_	SPI data input 2.
RB6/SCL1/SCK1	RB6	TTL	CMOS	General purpose I/O.
	SCL1	l ² C	OD	I ² C [™] clock 1.
	SCK1	ST	CMOS	SPI clock 1.
RB7/TX ^(1,2) /CK ^(1,2) /SCL2/SCK2	RB7	TTL	CMOS	General purpose I/O.
	ΤX	_	CMOS	USART asynchronous transmit.
	СК	ST	CMOS	USART synchronous clock.
	SCL2	l ² C	OD	l ² C [™] clock 2.
	SCK2	ST	CMOS	SPI clock 2.
RC0/AN4/CPS4/C2IN+/P1D ⁽¹⁾ /	RC0	TTL	CMOS	General purpose I/O.
<u>SS2^(1,2)</u>	AN4	AN		A/D Channel 4 input.
	CPS4	AN	_	Capacitive sensing input 4.
	C2IN+	AN		Comparator C2 positive input.
	P1D	_	CMOS	PWM output.
	SS2	ST	_	Slave Select input 2.
RC1/AN5/CPS5/C12IN1-/P1C ⁽¹⁾ /	RC1	TTL	CMOS	General purpose I/O.
SD02 ^(1,2)	AN5	AN	_	A/D Channel 5 input.
	CPS5	AN	_	Capacitive sensing input 5.
	C12IN1-	AN	_	Comparator C1 or C2 negative input.
	P1C	_	CMOS	PWM output.
	-			

TABLE 1-3:	PIC16F/LF1829 PINOUT DESCRIPTION (CONTINUED)

Legend:AN = Analog input or outputCMOS = CMOS compatible input or outputOD = Open DrainTTL = TTL compatible inputST = Schmitt Trigger input with CMOS levels l^2C^{TM} = Schmitt Trigger input with l^2C

HV = High Voltage XTAL = Crystal

I=C I™ = Schmitt Ti levels

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.

TABLE 1-3: PIC16F/LF1829 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC2/AN6/CPS6/C12IN2-/	RC2	TTL	CMOS	General purpose I/O.
P1D ^(1,2) /P2B ^(1,2) /MDCIN1	AN6	AN	_	A/D Channel 6 input.
	CPS6	AN	_	Capacitive sensing input 6.
	C12IN2-	AN		Comparator C1 or C2 negative input.
	P1D		CMOS	PWM output.
	P2B		CMOS	PWM output.
	MDCIN1	ST		Modulator Carrier Input 1.
RC3/AN7/CPS7/C12IN3-/	RC3	TTL	CMOS	General purpose I/O.
P2A ^(1,2) /CCP2 ^(1,2) /P1C ^(1,2) /	AN7	AN	_	A/D Channel 7 input.
MDMIN	CPS7	AN	_	Capacitive sensing input 7.
	C12IN3-	AN	_	Comparator C1 or C2 negative input.
	P2A	_	CMOS	PWM output.
	CCP2	AN	_	Capacitive sensing input 2.
	P1C	_	CMOS	PWM output.
	MDMIN	ST	_	Modulator source input.
RC4/C2OUT/SRNQ/P1B/TX ⁽¹⁾ /	RC4	TTL	CMOS	General purpose I/O.
CK ⁽¹⁾ /MDOUT	C2OUT	_	CMOS	Comparator C2 output.
	SRNQ	_	CMOS	SR Latch inverting output.
	P1B	_	CMOS	PWM output.
	TX	_	CMOS	USART asynchronous transmit.
	СК	ST	CMOS	USART synchronous clock.
	MDOUT	_	CMOS	Modulator output.
RC5/P1A/CCP1/DT ⁽¹⁾ /RX ⁽¹⁾ /	RC5	TTL	CMOS	General purpose I/O.
MDCIN2	P1A	_	CMOS	PWM output.
	CCP1	ST	CMOS	Capture/Compare/PWM 1.
	RX	ST	_	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	MDCIN2	ST	_	Modulator Carrier Input 2.
RC6/AN8/CPS8/CCP4/SS1	RC6	TTL	CMOS	General purpose I/O.
	AN8	AN	_	A/D Channel 8 input.
	CPS8	AN	_	Capacitive sensing input 8.
	CCP4	AN	_	Capacitive sensing input 4.
	SS1	ST		Slave Select input.
RC7/AN9/CPS9/SDO	RC7	TTL	CMOS	General purpose I/O.
	AN9	AN	_	A/D Channel 9 input.
	CPS9	AN		Capacitive sensing input 9.
	SDO	—	CMOS	SPI data output.
Vdd	Vdd	Power		Positive supply.
Vss	Vss	Power		Ground reference.

Legend:AN= Analog input or outputCMOS = CMOS compatible input or outputOD= Open DrainTTL = TTL compatible inputST= Schmitt Trigger input with CMOS levels I^2C^{TM} = Schmitt Trigger input with I²C

HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.

2: Default function location.

levels

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, indirect, and relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 8.5 "Automatic Context Saving"**, for more information.

2.2 16-level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See section **Section 3.4** "**Stack**" for more details.

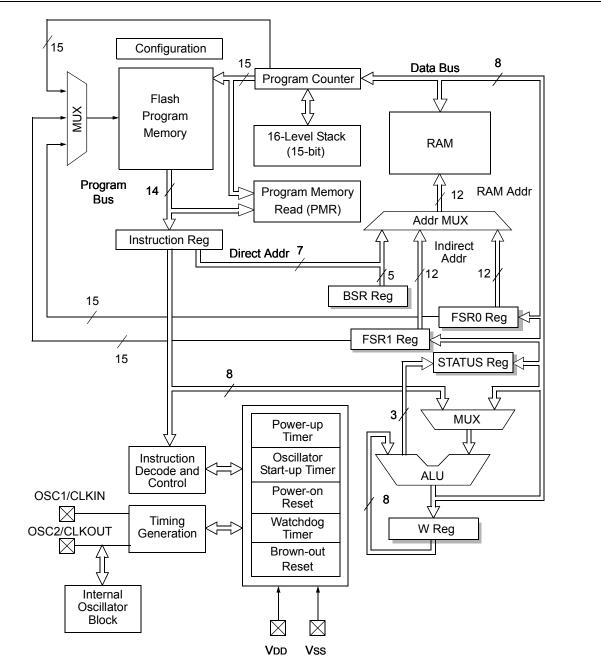
2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one data pointer for all memory. When an FSR points to program memory, there is 1 additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.5 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 29.0 "Instruction Set Summary**" for more details.





3.0 MEMORY ORGANIZATION

There are three types of memory in PIC16F/LF1825/1829 devices: Data Memory, Program Memory and Data EEPROM Memory⁽¹⁾.

- Program Memory
- Data Memory
 - Core Registers
 - Special Function Registers
 - General Purpose RAM
 - Common RAM
 - Device Memory Maps
 - Special Function Registers Summary
- Data EEPROM memory⁽¹⁾

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers is described in Section 11.0 "Data EEPROM and Flash Program Memory Control". The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16F/LF1825/1829 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h.

TABLE 3-1:DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address
PIC16F/LF1825/1829	8,192	7FFFh

FIGURE 3-1: **PROGRAM MEMORY MAP**

AND STACK FOR	
PIC16F/LF1825/1829	

		-
	PC<14:0>	
CAI RETUF Interru	RN, RETLW	
	Stack Level 0	
	Stack Level 1	_
	•	
	Stack Level 15	
	Reset Vector	10000h
	•	000011
	•	
(Interrupt Vector	0004h
	Page 0	0005h 07FFh
		0800h
	Page 1	
On-chip Program <	-	0FFFh
Memory	Page 2	1000h
		17FFh
	Page 3	1800h
		1FFFh
	Rollover to Page 0	2000h
	•	
	•	
	Rollover to Page 3	7FFFh

3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of ${\tt RETLW}$ instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 **RETLW** Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

constants	
BRW	;Add Index in W to
	;program counter to
	;select data
RETLW DATA0	;Index0 data
RETLW DATA1	;Index1 data
RETLW DATA2	
RETLW DATA3	
my_function	
; LOTS OF CODE	
MOVLW DATA_IN	IDEX
call constants	
; THE CONSTANT IS	IN W

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower 8 bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

constants			
RETLW	DATA0	;Index0	data
RETLW	DATA1	;Index1	data
RETLW	DATA2		
RETLW	data3		
my_functi	on		
; LO	IS OF CODE.		
MOVLW	LOW cons	stants	
MOVWF	FSR1L		
MOVLW	HIGH con	istants	
MOVWF	FSR1H		
MOVIW	0[FSR1]		
;THE PROG	RAM MEMORY	IS IN W	

3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-2):

- 12 core registers
- 20 Special Function Registers (SFR)
- · Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See Section 3.5 "Indirect Addressing" for more information.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation of the PIC16F/LF1825/1829. These registers are listed below:

- INDF0
- INDF1
- PCL
- STATUS
- FSR0 Low
- FSR0 High
- FSR1 Low
- FSR1 High
- BSR
- WREG
- PCLATH
- INTCON

Note: The core registers are the first 12 addresses of every data memory bank.

3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- · the arithmetic status of the ALU
- · the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

REGISTER 3-1: STATUS: STATUS REGISTER

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u uluu' (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to Section 29.0 "Instruction Set Summary").

Note 1:	The C and DC bits operate as Borrow
	and Digit Borrow out bits, respectively, in
	subtraction.

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u			
	— — <u>TO</u>				Z	DC ⁽¹⁾	C ⁽¹⁾			
bit 7		·		·		•	bit C			
Legend:										
R = Readable b	pit	W = Writable I	bit	U = Unimpler	nented bit, read	as '0'				
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Res							ther Resets			
'1' = Bit is set		'0' = Bit is clea	ared	q = Value depends on condition						

bit 7-5	Unimplemented: Read as '0'
bit 4	TO: Time-out bit
	1 = After power-up, CLRWDT instruction or SLEEP instruction 0 = A WDT time-out occurred
bit 3	PD: Power-down bit
	1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction
bit 2	Z: Zero bit
	 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
bit 1	DC: Digit Carry/Digit Borrow bit ⁽¹⁾
	 1 = A carry-out from the 4th low-order bit of the result occurred 0 = No carry-out from the 4th low-order bit of the result
bit 0	C: Carry/Borrow bit ⁽¹⁾
	 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred
Note 1	For Perrow the polarity is reversed. A subtraction is even ted by adding the two's complement of the

Note 1: For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

3.2.2 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.2.3 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank.

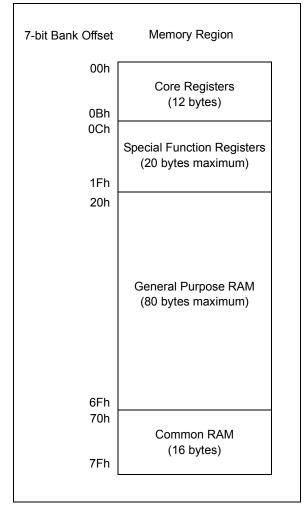
3.2.3.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.5.2** "Linear Data Memory" for more information.

3.2.4 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-2: BANKED MEMORY PARTITIONING



3.2.5 DEVICE MEMORY MAPS

The memory maps for the device family are as shown in Table 3-2.

TABLE 3-2: MEMORY MAP TABLES

Device	Banks	Table No.
PIC16F/LF1825/1829	0-7	Table 3-3
	8-15	Table 3-4
	16-23	Table 3-5
	24-31	Table 3-6
	31	Table 3-7

TABLE 3-3:PIC16F/LF1825/1829 MEMORY MAP, BANKS 0-7

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	INDF0	080h	INDF0	100h	INDF0	180h	INDF0	200h	INDF0	280h	INDF0	300h	INDF0	380h	INDF0
001h	INDF1	081h	INDF1	101h	INDF1	181h	INDF1	201h	INDF1	281h	INDF1	301h	INDF1	381h	INDF1
002h	PCL	082h	PCL	102h	PCL	182h	PCL	202h	PCL	282h	PCL	302h	PCL	382h	PCL
003h	STATUS	083h	STATUS	103h	STATUS	183h	STATUS	203h	STATUS	283h	STATUS	303h	STATUS	383h	STATUS
004h	FSR0L	084h	FSR0L	104h	FSR0L	184h	FSR0L	204h	FSR0L	284h	FSR0L	304h	FSR0L	384h	FSR0L
005h 006h	FSR0H FSR1L	085h 086h	FSR0H FSR1L	105h 106h	FSR0H FSR1L	185h 186h	FSR0H FSR1L	205h 206h	FSR0H FSR1L	285h 286h	FSR0H FSR1L	305h 306h	FSR0H FSR1L	385h 386h	FSR0H FSR1L
006h	FSR1L FSR1H	087h	FSR1L FSR1H	100h	FSR1L FSR1H	187h	FSR1L FSR1H	200n 207h	FSR1L	2001 287h	FSR1L	300n	FSR1L FSR1H	387h	FSR1L FSR1H
007h	BSR	088h	BSR	107h	BSR	188h	BSR	207h	BSR	288h	BSR	308h	BSR	388h	BSR
009h	WREG	089h	WREG	109h	WREG	189h	WREG	209h	WREG	289h	WREG	309h	WREG	389h	WREG
00Ah	PCLATH	08Ah	PCLATH	10Ah	PCLATH	18Ah	PCLATH	20Ah	PCLATH	28Ah	PCLATH	30Ah	PCLATH	38Ah	PCLATH
00Bh	INTCON	08Bh	INTCON	10Bh	INTCON	18Bh	INTCON	20Bh	INTCON	28Bh	INTCON	30Bh	INTCON	38Bh	INTCON
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	_	30Ch	_	38Ch	INLVLA
00Dh	PORTB ⁽¹⁾	08Dh	TRISB ⁽¹⁾	10Dh	LATB ⁽¹⁾	18Dh	ANSELB ⁽¹⁾	20Dh	WPUB ⁽¹⁾	28Dh	_	30Dh	_	38Dh	INLVLB ⁽¹⁾
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	_	30Eh	_	38Eh	INLVLC
00Fh		08Fh	_	10Fh	_	18Fh		20Fh	—	28Fh	_	30Fh	_	38Fh	_
010h		090h		110h	-	190h		210h	-	290h		310h	-	390h	—
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	EEADRL	211h	SSP1BUF	291h	CCPR1L	311h	CCPR3L	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	EEADRH	212h	SSP1ADD	292h	CCPR1H	312h	CCPR3H	392h	IOCAN
013h	—	093h		113h	CM2CON0	193h	EEDATL	213h	SSP1MSK	293h	CCP1CON	313h	CCP3CON	393h	IOCAF
014h	_	094h	_	114h	CM2CON1	194h	EEDATH	214h	SSP1STAT	294h	PWM1CON	314h		394h	IOCBP ⁽¹⁾
015h	TMR0	095h	OPTION	115h	CMOUT	195h	EECON1	215h	SSP1CON	295h	CCP1AS	315h	—	395h	IOCBN ⁽¹⁾
016h	TMR1L	096h	PCON	116h	BORCON	196h	EECON2	216h	SSP1CON2	296h	PSTR1CON	316h	—	396h	IOCBF ⁽¹⁾
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h		217h	SSP1CON3	297h		317h	—	397h	_
018h	T1CON	098h	OSCTUNE	118h	DACCON0	198h		218h		298h	CCPR2L	318h	CCPR4L	398h	_
019h	T1GCON	099h	OSCCON	119h	DACCON1	199h	RCREG	219h	SSP2BUF ⁽¹⁾	299h	CCPR2H	319h	CCPR4H	399h	_
01Ah	TMR2	09Ah	OSCSTAT	11Ah	SRCON0	19Ah	TXREG	21Ah	SSP2ADD ⁽¹⁾	29Ah	CCP2CON	31Ah	CCP4CON	39Ah	CLKRCON
01Bh	PR2	09Bh	ADRESL	11Bh	SRCON1	19Bh	SPBRGL	21Bh	SSP2MSK ⁽¹⁾	29Bh	PWM2CON	31Bh		39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	_	19Ch	SPBRGH	21Ch	SSP2STAT ⁽¹⁾	29Ch	CCP2AS	31Ch		39Ch	MDCON
01Dh		09Dh	ADCON0	11Dh	APFCON0	19Dh	RCSTA	21Dh	SSP2CON ⁽¹⁾	29Dh	PSTR2CON	31Dh	_	39Dh	MDSRC
01Eh	CPSCON0	09Eh	ADCON1	11Eh	APFCON1	19Eh	TXSTA	21Eh	SSP2CON2 ⁽¹⁾	29Eh	CCPTMRS	31Eh	_	39Eh	MDCARL
01Fh	CPSCON1	09Fh		11Fh		19Fh	BAUDCON	21Fh	SSP2CON3 ⁽¹⁾	29Fh	_	31Fh	—	39Fh	MDCARH
020h		0A0h		120h		1A0h		220h		2A0h		320h	General Purpose	3A0h	
	General		General Purpose Register	32Fh 330h	Register 16 Bytes ⁽²⁾		Unimplemented Read as '0'								
	Purpose Register		80 Bytes		80 Bytes		80 Bytes ⁽²⁾		80 Bytes ⁽²⁾		80 Bytes ⁽²⁾		Unimplemented Read as '0')	000	
06Fh	96 Bytes	0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
070h	,	0F0h	A	170h	A	1F0h		270h	A	2F0h	A	370h	A	3F0h	A = = 0.000
			Accesses 70h – 7Fh		Accesses 70h – 7Fh										
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

PIC16F/LF1825/1829

Legend: = Unimplemented data memory locations, read as '0'

Note 1: Available only on PIC16F/LF1829.

TABLE 3-4:PIC16F/LF1825/1829 MEMORY MAP, BANKS 8-15

	BANK 8		BANK 9		BANK 10	, D /	BANK 11		BANK 12		BANK 13		BANK 14		BANK 15
400h	INDF0	1 480h [INDF0	500h	INDF0	580h	INDF0	600h	INDF0	680h	INDF0	700h	INDF0	780h	INDF0
400h											-		-		
401h	INDF1	481h	INDF1 PCL	501h	INDF1 PCL	581h	INDF1	601h	INDF1 PCL	681h	INDF1	701h	INDF1 PCL	781h	INDF1 PCL
402h	PCL	482h		502h	-	582h	PCL	602h		682h	PCL	702h	-	782h	
403h	STATUS	483h	STATUS	503h	STATUS	583h	STATUS	603h	STATUS	683h	STATUS	703h	STATUS	783h	STATUS
404h	FSR0L FSR0H	484h	FSR0L FSR0H	504h	FSR0L FSR0H	584h	FSR0L FSR0H	604h	FSR0L FSR0H	684h	FSR0L FSR0H	704h	FSR0L FSR0H	784h	FSR0L
405h	FSR0H FSR1L	485h 486h	FSR0H FSR1L	505h	FSR0H FSR1L	585h 586h	FSR0H FSR1L	605h 606h	FSR0H FSR1L	685h 686h	FSR0H FSR1L	705h 706h	FSR0H FSR1L	785h 786h	FSR0H FSR1L
406h	FSR1L FSR1H	40011 487h	FSR1L FSR1H	506h	FSR1L FSR1H	587h	FSR1L FSR1H	607h	FSR1L FSR1H	687h	FSR1L FSR1H	700n 707h	FSR1L FSR1H	787h	FSR1L FSR1H
407h	BSR	487n 488h	BSR	507h	BSR	587h 588h	-		BSR	688h	-	707h 708h	BSR	787n 788h	BSR
408h	WREG	488n 489h	WREG	508h	WREG	588h 589h	BSR WREG	608h 609h	WREG	689h	BSR WREG	708n 709h	WREG	788n 789h	WREG
409h 40Ah	PCLATH	489n 48Ah	PCLATH	509h 50Ah	PCLATH	589n 58Ah	PCLATH	609h	PCLATH	689n 68Ah	PCLATH	709n 70Ah	PCLATH	789n 78Ah	PCLATH
40An 40Bh	INTCON	-	INTCON	50An 50Bh	INTCON		INTCON	60Bh	INTCON	68Bh	INTCON		INTCON	78Bh	INTCON
40Bh 40Ch		48Bh 48Ch		50Bh		58Bh 58Ch		60Bh		68Bh		70Bh 70Ch		78Bh 78Ch	
40Ch 40Dh		48Ch		50Ch		58Dh		60Dh		68Dh		70Ch		78Dh	
40Dh 40Eh		48Dh		50Dh		58Eh		60Eh		68Eh		70Dh 70Eh		78Eh	
40En 40Fh		40E∩ 48Fh		50En		58Fh		60Eh		68Fh		70En 70Fh		78Fh	
40FN 410h		40Fn 490h		50Fn 510h		590h		610h		690h		70Fn 710h		790h	
410h		490n 491h		510h		590h		611h		690h		710h		790h	
4110 412h		491h 492h		511n 512h		591n 592h		612h		692h		71111 712h		791n 792h	
4120 413h		49211 493h		512h		59211 593h		613h		693h		71211 713h		79211 793h	
413n 414h		493n 494h		513n 514h		593n 594h		614h		693n 694h		713n 714h		793n 794h	
414n 415h	 TMR4	4941 495h		514fi 515h		59411 595h		615h		695h		71411 715h		79411 795h	
4150 416h	PR4	495h 496h		515h		595h		616h		696h		715n 716h		795n 796h	_
4101 417h	T4CON	4901 497h	_	510h		590n 597h		617h		697h		717h		7901 797h	
41711 418h	14CON	49711 498h		517h		597h		618h		698h		718h		79711 798h	
4101 419h		498h		510h		590h		619h		699h		719h		7901 799h	
4190 41Ah		4990 49Ah		519h		5990 59Ah		61Ah		69Ah		71Ah		79911 79Ah	
41Bh		49Bh		51An 51Bh		59Bh		61Bh		69Bh		71Bh		79Bh	_
41Bh	 TMR6	49Bh 49Ch		51Ch		59Ch		61Ch		69Ch		71Ch		79DH	
41Dh	PR6	49Dh		51Dh		59Dh		61Dh		69Dh		71Dh		79Dh	
41Dh 41Eh	T6CON	49Dh		51Dh		59Dh		61Eh		69Eh		71Eh		79Dh 79Eh	
41En 41Fh		49En		51En		59En 59Fh		61Fh		69Eh		71En		79En 79Fh	
410 h	—	4A0h	_	520h	_	5A0h	_	620h		6A0h	_	720h		7A0h	—
12011	General	17 1011	General	02011	General	0/1011	General	02011		0, 1011		12011		77 1011	
	Purpose		Purpose		Purpose		Purpose		Unimplemented		Unimplemented		Unimplemented		Unimplemented
	Register		Register		Register		Register		Read as '0'		Read as '0'		Read as '0'		Read as '0'
	80 Bytes		80 Bytes		80 Bytes		80 Bytes								
46Fh	, -	4EFh	,	56Fh	,	5EFh		66Fh		6EFh		76Fh		7EFh	
470h		4F0h		570h		5F0h		670h		6F0h		770h		7F0h	
	Accesses		Accesses		Accesses		Accesses		Accesses		Accesses		Accesses		Accesses
	70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh						
17FL		1556		5756		EC.	/ / / / / /	6754		6EEk		7756	,	7656	/ // //
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

Legend: = Unimplemented data memory locations, read as '0'

TABLE 3-5: PIC16F/LF1825/1829 MEMORY MAP, BANKS 16-23

	BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23
800h	INDF0	880h	INDF0	900h	INDF0	980h	INDF0	A00h	INDF0	A80h	INDF0	B00h	INDF0	B80h	INDF0
801h	INDF1	881h	INDF1	901h	INDF1	981h	INDF1	A01h	INDF1	A81h	INDF1	B01h	INDF1	B81h	INDF1
802h	PCL	882h	PCL	902h	PCL	982h	PCL	A02h	PCL	A82h	PCL	B02h	PCL	B82h	PCL
803h	STATUS	883h	STATUS	903h	STATUS	983h	STATUS	A03h	STATUS	A83h	STATUS	B03h	STATUS	B83h	STATUS
804h	FSR0L	884h	FSR0L	904h	FSR0L	984h	FSR0L	A04h	FSR0L	A84h	FSR0L	B04h	FSR0L	B84h	FSR0L
805h	FSR0H	885h	FSR0H	905h	FSR0H	985h	FSR0H	A05h	FSR0H	A85h	FSR0H	B05h	FSR0H	B85h	FSR0H
806h	FSR1L	886h	FSR1L	906h	FSR1L	986h	FSR1L	A06h	FSR1L	A86h	FSR1L	B06h	FSR1L	B86h	FSR1L
807h	FSR1H	887h	FSR1H	907h	FSR1H	987h	FSR1H	A07h	FSR1H	A87h	FSR1H	B07h	FSR1H	B87h	FSR1H
808h	BSR	888h	BSR	908h	BSR	988h	BSR	A08h	BSR	A88h	BSR	B08h	BSR	B88h	BSR
809h	WREG	889h	WREG	909h	WREG	989h	WREG	A09h	WREG	A89h	WREG	B09h	WREG	B89h	WREG
80Ah	PCLATH	88Ah	PCLATH	90Ah	PCLATH	98Ah	PCLATH	A0Ah	PCLATH	A8Ah	PCLATH	B0Ah	PCLATH	B8Ah	PCLATH
80Bh	INTCON	88Bh	INTCON	90Bh	INTCON	98Bh	INTCON	A0Bh	INTCON	A8Bh	INTCON	B0Bh	INTCON	B8Bh	INTCON
80Ch	_	88Ch	—	90Ch		98Ch	_	A0Ch	—	A8Ch	_	B0Ch	_	B8Ch	—
80Dh	—	88Dh	_	90Dh	_	98Dh	_	A0Dh	—	A8Dh	—	B0Dh	—	B8Dh	_
80Eh	-	88Eh	_	90Eh		98Eh	-	A0Eh	—	A8Eh	-	B0Eh	-	B8Eh	—
80Fh	—	88Fh	—	90Fh	_	98Fh	_	A0Fh	—	A8Fh	—	B0Fh	—	B8Fh	—
810h		890h	—	910h		990h		A10h	—	A90h		B10h		B90h	—
811h		891h	_	911h		991h		A11h	—	A91h		B11h		B91h	—
812h	-	892h	—	912h		992h	_	A12h	—	A92h		B12h		B92h	—
813h	-	893h	—	913h		993h	_	A13h	—	A93h		B13h		B93h	—
814h	—	894h	—	914h	_	994h	_	A14h	—	A94h	—	B14h	—	B94h	—
815h	-	895h	_	915h		995h	-	A15h	—	A95h	-	B15h	-	B95h	—
816h	—	896h	—	916h	_	996h	_	A16h	—	A96h	—	B16h	—	B96h	—
817h	_	897h	_	917h	_	997h	_	A17h	_	A97h	_	B17h	_	B97h	_
818h	_	898h	_	918h	_	998h	_	A18h	_	A98h	_	B18h	_	B98h	_
819h	—	899h	_	919h	_	999h	_	A19h	_	A99h	—	B19h	—	B99h	_
81Ah	—	89Ah	_	91Ah	_	99Ah	_	A1Ah	_	A9Ah	—	B1Ah	—	B9Ah	_
81Bh	_	89Bh	_	91Bh	_	99Bh	_	A1Bh	—	A9Bh	—	B1Bh	—	B9Bh	_
81Ch	_	89Ch	_	91Ch	_	99Ch	_	A1Ch	_	A9Ch	_	B1Ch	_	B9Ch	_
81Dh	_	89Dh	_	91Dh	_	99Dh	_	A1Dh	_	A9Dh	_	B1Dh	_	B9Dh	_
81Eh	_	89Eh	_	91Eh	_	99Eh	_	A1Eh	_	A9Eh	_	B1Eh	_	B9Eh	_
81Fh	—	89Fh	—	91Fh	_	99Fh	_	A1Fh	_	A9Fh	—	B1Fh	—	B9Fh	_
820h		8A0h		920h		9A0h		A20h		AA0h		B20h		BA0h	
	Unimplemented Read as '0'														
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h		8F0h		970h		9F0h		A70h		AF0h		B70h		BF0h	
	Accesses 70h – 7Fh														
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-6: PIC16F/LF1825/1829 MEMORY MAP, BANKS 24-31

	BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31
C00h	INDF0	C80h	INDF0	D00h	INDF0	D80h	INDF0	E00h	INDF0	E80h	INDF0	F00h	INDF0	F80h	INDF0
C01h	INDF1	C81h	INDF1	D01h	INDF1	D81h	INDF1	E01h	INDF1	E81h	INDF1	F01h	INDF1	F81h	INDF1
C02h	PCL	C82h	PCL	D02h	PCL	D82h	PCL	E02h	PCL	E82h	PCL	F02h	PCL	F82h	PCL
C03h	STATUS	C83h	STATUS	D03h	STATUS	D83h	STATUS	E03h	STATUS	E83h	STATUS	F03h	STATUS	F83h	STATUS
C04h	FSR0L	C84h	FSR0L	D04h	FSR0L	D84h	FSR0L	E04h	FSR0L	E84h	FSR0L	F04h	FSR0L	F84h	FSR0L
C05h	FSR0H	C85h	FSR0H	D05h	FSR0H	D85h	FSR0H	E05h	FSR0H	E85h	FSR0H	F05h	FSR0H	F85h	FSR0H
C06h	FSR1L	C86h	FSR1L	D06h	FSR1L	D86h	FSR1L	E06h	FSR1L	E86h	FSR1L	F06h	FSR1L	F86h	FSR1L
C07h	FSR1H	C87h	FSR1H	D07h	FSR1H	D87h	FSR1H	E07h	FSR1H	E87h	FSR1H	F07h	FSR1H	F87h	FSR1H
C08h	BSR	C88h	BSR	D08h	BSR	D88h	BSR	E08h	BSR	E88h	BSR	F08h	BSR	F88h	BSR
C09h	WREG	C89h	WREG	D09h	WREG	D89h	WREG	E09h	WREG	E89h	WREG	F09h	WREG	F89h	WREG
C0Ah	PCLATH	C8Ah	PCLATH	D0Ah	PCLATH	D8Ah	PCLATH	E0Ah	PCLATH	E8Ah	PCLATH	F0Ah	PCLATH	F8Ah	PCLATH
C0Bh	INTCON	C8Bh	INTCON	D0Bh	INTCON	D8Bh	INTCON	E0Bh	INTCON	E8Bh	INTCON	F0Bh	INTCON	F8Bh	INTCON
C0Ch	—	C8Ch	_	D0Ch	_	D8Ch	_	E0Ch	_	E8Ch	—	F0Ch	—	F8Ch	
C0Dh	—	C8Dh	_	D0Dh	_	D8Dh	_	E0Dh	_	E8Dh	—	F0Dh	—	F8Dh	
C0Eh	—	C8Eh	_	D0Eh	_	D8Eh	—	E0Eh	—	E8Eh	_	F0Eh	—	F8Eh	
C0Fh	_	C8Fh	_	D0Fh	_	D8Fh	_	E0Fh	_	E8Fh	_	F0Fh	—	F8Fh	
C10h	_	C90h	_	D10h	_	D90h	_	E10h	_	E90h	_	F10h	—	F90h	
C11h	_	C91h		D11h		D91h	—	E11h	—	E91h	_	F11h	_	F91h	
C12h	_	C92h	-	D12h	-	D92h	—	E12h	—	E92h	_	F12h	-	F92h	
C13h	—	C93h	—	D13h	—	D93h	—	E13h	—	E93h	—	F13h	—	F93h	
C14h	—	C94h	—	D14h	—	D94h	—	E14h	—	E94h	—	F14h	—	F94h	
C15h	—	C95h	_	D15h	_	D95h	—	E15h	—	E95h	_	F15h	—	F95h	
C16h		C96h		D16h		D96h	—	E16h	—	E96h		F16h		F96h	
C17h	_	C97h	_	D17h	_	D97h	_	E17h	_	E97h	_	F17h	—	F97h	See Table 3-7 for
C18h	_	C98h	_	D18h	_	D98h	_	E18h	_	E98h	_	F18h	—	F98h	register mapping
C19h	—	C99h	_	D19h	_	D99h	_	E19h	_	E99h	—	F19h	—	F99h	details
C1Ah	—	C9Ah	_	D1Ah	_	D9Ah	_	E1Ah	_	E9Ah	—	F1Ah	—	F9Ah	
C1Bh	—	C9Bh	_	D1Bh	_	D9Bh	_	E1Bh	_	E9Bh	—	F1Bh	—	F9Bh	
C1Ch	_	C9Ch	_	D1Ch	_	D9Ch	_	E1Ch	_	E9Ch	_	F1Ch	—	F9Ch	
C1Dh	_	C9Dh	_	D1Dh	_	D9Dh	_	E1Dh	_	E9Dh	_	F1Dh	—	F9Dh	
C1Eh	_	C9Eh	_	D1Eh	_	D9Eh	_	E1Eh	_	E9Eh	_	F1Eh	—	F9Eh	
C1Fh	_	C9Fh	_	D1Fh	_	D9Fh	_	E1Fh	_	E9Fh	_	F1Fh	—	F9Fh	
C20h		CA0h		D20h		DA0h		E20h		EA0h		F20h		FA0h	
	Unimplemented Read as '0'														
C6Fh		CEFh		D6Fh		DEFh		E6Fh		EEFh		F6Fh		FEFh	
C70h		CF0h		D70h		DF0h		E70h		EF0h		F70h		FF0h	
	Accesses 70h – 7Fh		Accesses 70h – 7Fh												
CFFh		CFFh		D7Fh		DFFh		E7Fh		EFFh		F7Fh		FFFh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-7:PIC16F/LF1825/1829 MEMORY
MAP, BANK 31

		Bank 31 ⁽¹⁾	
	F8Ch		
		Unimplemented Read as '0'	
	FE3h		
	FE4h	STATUS_SHAD	
	FE5h	WREG_SHAD	
	FE6h	BSR_SHAD	
	FE7h	PCLATH_SHAD	
	FE8h	FSR0L_SHAD	
	FE9h	FSR0H_SHAD	
	FEAh	FSR1L_SHAD	
	FEBh	FSR1H_SHAD	
	FECh	—	
	FEDh	STKPTR	
	FEEh	TOSL	
	FEFh	TOSH	
Lege		= Unimplemented da read as '0'.	ta memory locations,

3.2.6 SPECIAL FUNCTION REGISTERS SUMMARY

The Special Function Register summary for the device family are as follows:

Device	Bank(s)	Page No.
	0	33
	1	34
	2	35
	3	36
	4	37
PIC16F/LF1825/1829	5	38
	6	39
	7	40
	8	41
	9-30	42
	31	43

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 0											
000h ⁽¹⁾	INDF0	Addressing th (not a physica		es contents of	FSR0H/FSR0)L to address	data memory	1		XXXX XXXX	****
001h ⁽¹⁾	INDF1	Addressing th (not a physical		es contents of	FSR1H/FSR1	L to address	data memory	1		****	****
002h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant E	Byte					0000 0000	0000 0000
003h ⁽¹⁾	STATUS	_	—	—	TO	PD	Z	DC	С	1 1000	q quuu
004h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poir	nter	•		•	•	0000 0000	uuuu uuuu
005h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Poi	nter					0000 0000	0000 0000
006h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poir	nter					0000 0000	uuuu uuuu
007h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Poi	nter					0000 0000	0000 0000
008h ⁽¹⁾	BSR	_	_	_			BSR<4:0>			0 0000	0 0000
009h ⁽¹⁾	WREG	Working Reg	ister	•	•					0000 0000	uuuu uuuu
00Ah ⁽¹⁾	PCLATH	_	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	r			-000 0000	-000 0000
00Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
00Ch	PORTA	_	_	RA5	RA4	RA3	RA2	RA1	RA0	xx xxxx	xx xxxx
00Dh	PORTB ⁽²⁾	RB7	RB6	RB5	RB4	_	_	_	_	xxxx	xxxx
00Eh	PORTC	RC7 ⁽²⁾	RC6 ⁽²⁾	RC5	RC4	RC3	RC2	RC1	RC0	XXXX XXXX	XXXX XXXX
00Fh	—	Unimplement	ed							_	_
010h	—	Unimplement	ed							_	_
011h	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
012h	PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	0000 00	0000 00
013h	PIR3	_	_	CCP4IF	CCP3IF	TMR6IF	_	TMR4IF	_	00 0-0-	00 0-0-
014h	PIR4 ⁽²⁾	_	—	—	_	_	_	BCL2IF	SSP2IF	00	00
015h	TMR0	Timer0 Modu	le Register							XXXX XXXX	uuuu uuuu
016h	TMR1L	Holding Regi	ster for the Le	ast Significant	Byte of the 16	6-bit TMR1 Re	egister			XXXX XXXX	uuuu uuuu
017h	TMR1H	Holding Regi	ster for the Mo	ost Significant I	Byte of the 16	-bit TMR1 Re	gister			XXXX XXXX	uuuu uuuu
018h	T1CON	TMR1CS1	TMR1CS0	T1CKP	S<1:0>	T10SCEN	T1SYNC	—	TMR10N	0000 00-0	uuuu uu-u
019h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T <u>1GGO</u> / DONE	T1GVAL	T1GS	S<1:0>	0000 0x00	uuuu uxuu
01Ah	TMR2	Timer2 Modu	le Register	•	•		•	•		0000 0000	0000 0000
01Bh	PR2	Timer2 Perio	d Register							1111 1111	1111 1111
01Ch	T2CON	-		T2OUTF	PS<3:0>		TMR2ON	T2CKP	S<1:0>	-000 0000	-000 0000
01Dh	—	Unimplement	ed							-	-
01Eh	CPSCON0	CPSON	CPSRM	_	_	CPSRN	G<1:0>	CPSOUT	T0XCS	00 0000	00 0000
01Fh	CPSCON1	_	_	_	_		CPSCI	H<3:0>		0000	0000

TABLE 3-8: SPECIAL FUNCTION REGISTER SUMMARY
--

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: PIC16F/LF1829 only.

3: PIC16F/LF1825 only.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 1											
080h ⁽¹⁾	INDF0	Addressing th (not a physical		es contents of	FSR0H/FSR0	L to address	data memory	,		****	****
081h ⁽¹⁾	INDF1	Addressing th (not a physical		es contents of	FSR1H/FSR1	L to address	data memory	,		****	XXXX XXXX
082h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant E	Byte					0000 0000	0000 0000
083h ⁽¹⁾	STATUS	_	_	_	TO	PD	Z	DC	С	1 1000	q quuu
084h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poir	nter					0000 0000	uuuu uuuu
085h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Poi	nter					0000 0000	0000 0000
086h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poir	nter					0000 0000	uuuu uuuu
087h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Poi	nter					0000 0000	0000 0000
088h ⁽¹⁾	BSR	—	_	—			BSR<4:0>			0 0000	0 0000
089h ⁽¹⁾	WREG	Working Reg	ister							0000 0000	uuuu uuuu
08Ah ⁽¹⁾	PCLATH	—	Write Buffer f	or the upper 7	bits of the Pro	gram Counte	r			-000 0000	-000 0000
08Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
08Ch	TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	11 1111	11 1111
08Dh	TRISB ⁽²⁾	TRISB7	TRISB6	TRISB5	TRISB4	_	_	_	_	1111	1111
08Eh	TRISC	TRISC7 ⁽²⁾	TRISC6 ⁽²⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
08Fh	—	Unimplement	ed							_	_
090h	—	Unimplement	ed							_	_
091h	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
092h	PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	_	_	CCP2IE	0000 00	0000 00
093h	PIE3	_	_	CCP4IE	CCP3IE	TMR6IE	_	TMR4IE	_	00 0-0-	00 0-0-
094h	PIE4 ⁽²⁾	_	_	_	_	_	_	BCL2IE	SSP2IE	00	00
095h	OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA		PS<2:0>		1111 1111	1111 1111
096h	PCON	STKOVF	STKUNF	_	_	RMCLR	RI	POR	BOR	00 11qq	qq qquu
097h	WDTCON	_	_		V	VDTPS<4:0>			SWDTEN	01 0110	01 0110
098h	OSCTUNE	_	_			TUN<	5:0>			00 0000	00 0000
099h	OSCCON	SPLLEN		IRCF<	<3:0>		_	SCS	<1:0>	0011 1-00	0011 1-00
09Ah	OSCSTAT	T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	10q0 0q00	dddd ddod
09Bh	ADRESL	A/D Result R	egister Low							XXXX XXXX	uuuu uuuu
09Ch	ADRESH	A/D Result R	egister High							XXXX XXXX	սսսս սսսս
09Dh	ADCON0	_			CHS<4:0>			GO/DONE	ADON	-000 0000	-000 0000
09Eh	ADCON1	ADFM		ADCS<2:0>		_	ADNREF	ADPRE	F<1:0>	0000 -000	0000 -000
			I				I	I			

SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED) **TABLE 3-8:**

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

PIC16F/LF1829 only.
 PIC16F/LF1825 only.

DS41440A-page 34

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 2											
100h ⁽¹⁾	INDF0	Addressing the (not a physic)		es contents of	FSR0H/FSR0	L to address	data memory	/		XXXX XXXX	XXXX XXXX
101h ⁽¹⁾	INDF1	Addressing the (not a physic)		es contents of	FSR1H/FSR1	L to address	data memory	/		XXXX XXXX	XXXX XXXX
102h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant B	lyte					0000 0000	0000 0000
103h ⁽¹⁾	STATUS	_	_	_	TO	PD	Z	DC	С	1 1000	q quuu
104h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poir	nter					0000 0000	uuuu uuuu
105h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Poi	nter					0000 0000	0000 0000
106h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poir	nter					0000 0000	uuuu uuuu
107h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Poi	nter					0000 0000	0000 0000
108h ⁽¹⁾	BSR	_	—	—			BSR<4:0>			0 0000	0 0000
109h ⁽¹⁾	WREG	Working Reg	ister							0000 0000	սսսս սսսս
10Ah ⁽¹⁾	PCLATH	_	Write Buffer f	or the upper 7	bits of the Pro	gram Counte	er			-000 0000	-000 0000
10Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
10Ch	LATA	_	—	LATA5	LATA4	_	LATA2	LATA1	LATA0	xx -xxx	uu -uuu
10Dh	LATB ⁽²⁾	LATB7	LATB6	LATB5	LATB4	_	—	_	_	xxxx	xxxx
10Eh	LATC	LATC7 ⁽²⁾	LATC6 ⁽²⁾	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	XXXX XXXX	uuuu uuuu
10Fh	—	Unimplement	ted							_	
110h	—	Unimplement	ted							-	_
111h	CM1CON0	C10N	C10UT	C10E	C1POL	_	C1SP	C1HYS	C1SYNC	0000 -100	0000 -100
112h	CM1CON1	C1INTP	C1INTN	C1PCF	1<1:0>	_	_	C1NCH1	C1NCH0	00000	00000
113h	CM2CON0	C2ON	C2OUT	C2OE	C2POL	_	C2SP	C2HYS	C2SYNC	0000 -100	0000 -100
114h	CM2CON1	C2INTP	C2INTN	C2PCH	1<1:0>	_	_	C2NCH	H<1:0>	000000	000000
115h	CMOUT	_	_	_	_	_	_	MC2OUT	MC1OUT	00	00
116h	BORCON	SBOREN	_	_	_	_	_	_	BORRDY	1 q	u u
117h	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFV	'R<1:0>	ADFVF	R<1:0>	0000 00p0	0q00 0000
118h	DACCON0	DACEN	DACLPS	DACOE	—	DACPS	S<1:0>	_	DACNSS	000- 00-0	000- 00-0
119h	DACCON1	_	_	_			DACR<4:0>			0 0000	0 0000
11Ah	SRCON0	SRLEN		SRCLK<2:0>		SRQEN	SRNQEN	SRPS	SRPR	0000 0000	0000 0000
11Bh	SRCON1	SRSPE	SRSCKE	SRSC2E ⁽²⁾	SRSC1E	SRRPE	SRRCKE	SRRC2E ⁽²⁾	SRRC1E	0000 0000	0000 0000
11Ch	_	Unimplement	ted							—	
11Dh	APFCON0	RXDTSEL	SDOSEL ⁽³⁾	SSSEL ⁽³⁾	_	T1GSEL	TXCKSEL			000- 0000	000- 0000
11Eh	APFCON1	_		SDO2SEL ⁽²⁾	SS2SEL ⁽²⁾	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	00 0000	00 0000
11Fh	_	Unimplement	ted							_	

TABLE 3-8: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: PIC16F/LF1829 only.

3: PIC16F/LF1825 only.

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 3											
180h ⁽¹⁾	INDF0	Addressing the (not a physic)		es contents of	FSR0H/FSR0	L to address	data memory	/		XXXX XXXX	****
181h ⁽¹⁾	INDF1	Addressing the (not a physic)		es contents of	FSR1H/FSR1	L to address	data memory	/		XXXX XXXX	XXXX XXXX
182h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant E	Byte					0000 0000	0000 0000
183h ⁽¹⁾	STATUS	—	_	_	TO	PD	Z	DC	С	1 1000	q quuu
184h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poir	nter					0000 0000	uuuu uuuu
185h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Poi	inter					0000 0000	0000 0000
186h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poir	nter					0000 0000	uuuu uuuu
187h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Poi	inter					0000 0000	0000 0000
188h ⁽¹⁾	BSR	_	_	_			BSR<4:0>			0 0000	0 0000
189h ⁽¹⁾	WREG	Working Reg	ister							0000 0000	uuuu uuuu
18Ah ⁽¹⁾	PCLATH	—	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	r			-000 0000	-000 0000
18Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
18Ch	ANSELA	—	_	_	ANSA4	—	ANSA2	ANSA1	ANSA0	1 -111	1 -111
18Dh	ANSELB ⁽²⁾	ANSB7	ANSB6	ANSB5	ANSB4	_	_	_	_	1111	1111
18Eh	ANSELC	ANSC7 ⁽²⁾	ANSC6 ⁽²⁾	-	_	ANSC3	ANSC2	ANSC1	ANSC0	11 1111	11 1111
18Fh	—	Unimplement	ed		•	•		•	•	—	_
190h	—	Unimplement	ed							_	_
191h	EEADRL	EEPROM / P	rogram Memo	ry Address Re	gister Low By	te				0000 0000	0000 0000
192h	EEADRH	—	EEPROM / P	rogram Memo	ry Address Re	gister High B	yte			-000 0000	-000 0000
193h	EEDATL	EEPROM / P	rogram Memo	ry Read Data	Register Low	Byte				XXXX XXXX	uuuu uuuu
194h	EEDATH	_	_	EEPROM / PI	rogram Memo	ry Read Data	Register Hig	gh Byte		xx xxxx	uu uuuu
195h	EECON1	EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	0000 x000	0000 q000
196h	EECON2	EEPROM co	ntrol register 2							0000 0000	0000 0000
197h	—	Unimplement	ed							_	_
198h	—	Unimplement	ed							_	_
199h	RCREG	USART Rece	ive Data Regi	ster						0000 0000	0000 0000
19Ah	TXREG	USART Trans	smit Data Reg	ister						0000 0000	0000 0000
19Bh	SPBRGL	Baud Rate G	enerator Data	Register Low						0000 0000	0000 0000
19Ch	SPBRGH	Baud Rate G	enerator Data	Register High						0000 0000	0000 0000
19Dh	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19Eh	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
	BAUDCON	ABDOVF	RCIDL		SCKP	BRG16		WUE	ABDEN	01-0 0-00	01-0 0-00

SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED) TABLE 3-8

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: These registers can be addressed from any bank.

PIC16F/LF1829 only.
 PIC16F/LF1825 only.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 4											
200h ⁽¹⁾	INDF0	Addressing th (not a physic		es contents of	FSR0H/FSR0	L to address	data memory	/		XXXX XXXX	XXXX XXXX
201h ⁽¹⁾	INDF1	Addressing th (not a physic		es contents of	FSR1H/FSR1	L to address	data memory	/		XXXX XXXX	XXXX XXXX
202h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant E	lyte					0000 0000	0000 0000
203h ⁽¹⁾	STATUS	—	—	—	TO	PD	Z	DC	С	1 1000	q quuu
204h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poir	nter	•		•	•	0000 0000	uuuu uuuu
205h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Poi	nter					0000 0000	0000 0000
206h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poir	nter					0000 0000	uuuu uuuu
207h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Poi	nter					0000 0000	0000 0000
208h ⁽¹⁾	BSR	_	_	—			BSR<4:0>			0 0000	0 0000
209h ⁽¹⁾	WREG	Working Reg	ister		•					0000 0000	uuuu uuuu
20Ah ⁽¹⁾	PCLATH	_	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	r			-000 0000	-000 0000
20Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
20Ch	WPUA	_	_	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	11 1111	11 1111
20Dh	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	_	_	_	—	1111	1111
20Eh	WPUC	WPUC7 ⁽²⁾	/PUC7 ⁽²⁾ WPUC6 ⁽²⁾ WPUC5 WPUC4 WPUC3 WPUC2 WPUC1 WPUC0 1							1111 1111	1111 1111
20Fh	—	Unimplement	nimplemented						_		
210h	—	Unimplement	ted							_	
211h	SSP1BUF	Synchronous	Serial Port Re	eceive Buffer/T	ransmit Regis	ster				XXXX XXXX	uuuu uuuu
212h	SSP1ADD		ADD<7:0>					0000 0000	0000 0000		
213h	SSP1MSK				MSK<7	/:0>				1111 1111	1111 1111
214h	SSP1STAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000
215h	SSP1CON1	WCOL	SSPOV	SSPEN	CKP		SSPN	1<3:0>		0000 0000	0000 0000
216h	SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
217h	SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000 0000	0000 0000
218h	—	Unimplement	ted							_	_
219h	SSP2BUF ⁽²⁾	Synchronous	Serial Port Re	eceive Buffer/T	ransmit Regis	ster				XXXX XXXX	uuuu uuuu
21Ah	SSP2ADD ⁽²⁾				ADD<7	:0>				0000 0000	0000 0000
21Bh	SSP2MSK ⁽²⁾				MSK<7	/:0>				1111 1111	1111 1111
21Ch	SSP2STAT ⁽²⁾	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000
21Dh	SSP2CON1(2)	WCOL	SSPOV	SSPEN	CKP		SSPM	1<3:0>		0000 0000	0000 0000
21Eh	SSP2CON2(2)	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
21Fh	SSP2CON3(2)	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000 0000	0000 0000

TABLE 3-8 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

 ${\rm x}$ = unknown, ${\rm u}$ = unchanged, ${\rm q}$ = value depends on condition, - = unimplemented, ${\rm r}$ = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: These registers can be addressed from any bank.

2: PIC16F/LF1829 only.

3: PIC16F/LF1825 only.

	3-8: 5			REGIST							
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 5											
280h ⁽¹⁾	INDF0	Addressing th (not a physical		es contents of	FSR0H/FSR0	L to address	data memory	1		****	XXXX XXXX
281h ⁽¹⁾	INDF1	Addressing th (not a physical		es contents of	FSR1H/FSR1	L to address	data memory	1		****	****
282h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant E	Byte					0000 0000	0000 0000
283h ⁽¹⁾	STATUS	—	_	_	TO	PD	Z	DC	С	1 1000	q quuu
284h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poi	nter	•	•	•	•	0000 0000	uuuu uuuu
285h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Po	inter					0000 0000	0000 0000
286h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poi	nter					0000 0000	uuuu uuuu
287h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Po	inter					0000 0000	0000 0000
288h ⁽¹⁾	BSR	_	_	_			BSR<4:0>			0 0000	0 0000
289h ⁽¹⁾	WREG	Working Reg	ister							0000 0000	uuuu uuuu
28Ah ⁽¹⁾	PCLATH	_	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	er			-000 0000	-000 0000
28Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
28Ch	_	Unimplement	ed						•	_	_
28Dh	_	Unimplement	ed							_	_
28Eh	_	Unimplement	nimplemented						_	_	
28Fh	_	Unimplement	Inimplemented					_	_		
290h	_	Unimplement	nimplemented					_	_		
291h	CCPR1L	Capture/Com	apture/Compare/PWM Register 1 (LSB)					XXXX XXXX	uuuu uuuu		
292h	CCPR1H	Capture/Com						XXXX XXXX	uuuu uuuu		
293h	CCP1CON	P1M	<1:0>	DC1E	8<1:0>		CCP1N	√<3:0>		0000 0000	0000 0000
294h	PWM1CON	P1RSEN			F	P1DC<6:0>				0000 0000	0000 0000
295h	CCP1AS	CCP1ASE		CCP1AS<2:0>	>	PSS1A	.C<1:0>	PSS1B	D<1:0>	0000 0000	0000 0000
296h	PSTR1CON	_	_	_	STR1SYNC	STR1D	STR1C	STR1B	STR1A	0 0001	0 0001
297h	_	Unimplement	ed						•	_	_
298h	CCPR2L	Capture/Com	pare/PWM Re	egister 2 (LSB))					XXXX XXXX	uuuu uuuu
299h	CCPR2H	Capture/Com	pare/PWM Re	egister 2 (MSB	5)					XXXX XXXX	uuuu uuuu
29Ah	CCP2CON	P2M1	P2M0	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	0000 0000	0000 0000
29Bh	PWM2CON	P2RSEN	P2DC6	P2DC5	P2DC4	P2DC3	P2DC2	P2DC1	P2DC0	0000 0000	0000 0000
29Ch	CCP2AS	CCP2ASE	CCP2AS2	CCP2AS1	CCP2AS0	PSS2AC1	PSS2AC0	PSS2BD1	PSS2BD0	0000 0000	0000 0000
29Dh	PSTR2CON	—	—	—	STR2SYNC	STR2D	STR2C	STR2B	STR2A	0 0001	0 0001
29Eh	CCPTMRS	C4TSEL1	C4TSEL0	C3TSEL1	C3TSEL0	C2TSEL1	C2TSEL0	C1TSEL1	C1TSEL0	0000 0000	0000 0000
		Unimplement		•			•		•	1	

SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED) **TABLE 3-8:**

 ${\rm x}$ = unknown, u = unchanged, ${\rm q}$ = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: These registers can be addressed from any bank.

PIC16F/LF1829 only.
 PIC16F/LF1825 only.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 6											
300h ⁽¹⁾	INDF0	Addressing the (not a physic)		es contents of	FSR0H/FSR0)L to address	data memory	/		XXXX XXXX	XXXX XXXX
301h ⁽¹⁾	INDF1	Addressing the (not a physic)		es contents of	FSR1H/FSR1	L to address	data memory	/		XXXX XXXX	XXXX XXXX
302h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant E	3yte					0000 0000	0000 0000
303h ⁽¹⁾	STATUS	—	—	—	TO	PD	Z	DC	С	1 1000	q quuu
304h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poir	nter					0000 0000	uuuu uuuu
305h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Poi	nter					0000 0000	0000 0000
306h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poir	nter					0000 0000	uuuu uuuu
307h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Poi	nter					0000 0000	0000 0000
308h ⁽¹⁾	BSR	_	—	—			BSR<4:0>			0 0000	0 0000
309h ⁽¹⁾	WREG	Working Reg	ister							0000 0000	uuuu uuuu
30Ah ⁽¹⁾	PCLATH	_	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	er			-000 0000	-000 0000
30Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
30Ch	—	Unimplement	ed							_	_
30Dh	—	Unimplement	ed							_	_
30Eh	—	Unimplement	nimplemented						_	_	
30Fh	—	Unimplement	ed							_	_
310h	—	Unimplement	ed							_	_
311h	CCPR3L	Capture/Com	pare/PWM Re	gister 3 (LSB)						XXXX XXXX	uuuu uuuu
312h	CCPR3H	Capture/Com	pare/PWM Re	gister 3 (MSB)					XXXX XXXX	uuuu uuuu
313h	CCP3CON	_	—	DC3B1	DC3B0	CCP3M3	CCP3M2	CCP3M1	CCP3M0	00 0000	00 0000
314h	—	Unimplement	ed							_	_
315h	—	Unimplement	ed							_	_
316h	—	Unimplement	ed							_	_
317h	—	Unimplement	ed							_	_
318h	CCPR4L	Capture/Com	pare/PWM Re	egister 4 (LSB)						XXXX XXXX	uuuu uuuu
319h	CCPR4H	Capture/Com	pare/PWM Re	gister 4 (MSB)					XXXX XXXX	uuuu uuuu
31Ah	CCP4CON	—	_	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	00 0000	00 0000
31Bh	—	Unimplement	ed							_	_
31Ch	—	Unimplement	ed							_	—
31Dh	—	Unimplement	ed							_	—
31Eh	—	Unimplement	ed							_	—
		1	ed							1	

TABLE 3-8 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

 ${\rm x}$ = unknown, ${\rm u}$ = unchanged, ${\rm q}$ = value depends on condition, - = unimplemented, ${\rm r}$ = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: These registers can be addressed from any bank.

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 7											
380h ⁽¹⁾	INDF0	Addressing the (not a physic)		es contents of	FSR0H/FSR0	L to address	data memory	/		XXXX XXXX	XXXX XXXX
381h ⁽¹⁾	INDF1	Addressing the (not a physic)		es contents of	FSR1H/FSR1	L to address	data memory	/		XXXX XXXX	XXXX XXXX
382h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant B	lyte					0000 0000	0000 0000
383h ⁽¹⁾	STATUS	—	—	—	TO	PD	Z	DC	С	1 1000	q quuu
384h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poir	nter	•		•	•	0000 0000	uuuu uuuu
385h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Poi	nter					0000 0000	0000 0000
386h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poir	nter					0000 0000	uuuu uuuu
387h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Poi	nter					0000 0000	0000 0000
388h ⁽¹⁾	BSR	—	—	—			BSR<4:0>			0 0000	0 0000
389h ⁽¹⁾	WREG	Working Reg	ister							0000 0000	uuuu uuuu
38Ah ⁽¹⁾	PCLATH	_	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	r			-000 0000	-000 0000
38Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 0000
38Ch	INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	00 0100	00 0100
38Dh	INLVLB ⁽²⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	_	_	_	_	0000	0000
38Eh	INLVLC	INLVLC7 ⁽²⁾	INLVLC6(2)	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	11xx xxxx	11xx xxxx
38Fh	_	Unimplement	ed					•	•	_	_
390h	—	Unimplement	•						_	_	
391h	IOCAP	_	_	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	00 0000	00 0000
392h	IOCAN	_	_	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	00 0000	00 0000
393h	IOCAF	_	_	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	00 0000	00 0000
394h	IOCBP ⁽²⁾	IOCBP7	IOCBP6	IOCBP5	IOCBP4	_	_	_	_	0000	0000
395h	IOCBN ⁽²⁾	IOCBN7	IOCBN6	IOCBN5	IOCBN4	_	_	_	_	0000	0000
396h	IOCBF ⁽²⁾	IOCBF7	IOCBF6	IOCBF5	IOCBF4	_	_	_	_	0000	0000
397h	_	Unimplement	ed							_	_
398h	_	Unimplement	ed							_	_
399h	_	Unimplement	ed							_	_
39Ah	CLKRCON	CLKREN	CLKROE	CLKRSLR	CLKRD	C<1:0>	(CLKRDIV<2:0	>	0011 0000	0011 0000
39Bh	—	Unimplement	ed							_	—
39Ch	MDCON	MDEN	MDOE	MDSLR	MDOPOL	MDOUT		_	MDBIT	00100	00100
39Dh	MDSRC	MDMSODIS	—	—	—		MDMS	5<3:0>		x xxxx	u uuuu
39Eh	MDCARL	MDCLODIS	MDCLPOL	MDCLSYNC	_		MDCL	_<3:0>		xxx- xxxx	uuu- uuuu
39Fh	MDCARH	MDCHODIS	MDCHPOL	MDCHSYNC	_					xxx- xxxx	uuu- uuuu

SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED) TABLE 3-8

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: These registers can be addressed from any bank.

PIC16F/LF1829 only.
 PIC16F/LF1825 only.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 8							•				
400h ⁽¹⁾	INDF0	Addressing th (not a physic		es contents of	FSR0H/FSR0)L to address	data memory	,		XXXX XXXX	XXXX XXXX
401h ⁽¹⁾	INDF1	Addressing the (not a physic)		es contents of	FSR1H/FSR1	L to address	data memory	,		XXXX XXXX	XXXX XXXX
402h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant E	Byte					0000 0000	0000 0000
403h ⁽¹⁾	STATUS	—	_	—	TO	PD	Z	DC	С	1 1000	q quuu
404h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poir	nter	•	•			0000 0000	uuuu uuuu
405h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Poi	inter					0000 0000	0000 0000
406h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poir	nter					0000 0000	uuuu uuuu
407h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Poi	inter					0000 0000	0000 0000
408h ⁽¹⁾	BSR	_	—	—			BSR<4:0>			0 0000	0 0000
409h ⁽¹⁾	WREG	Working Reg	ister							0000 0000	սսսս սսսս
40Ah ⁽¹⁾	PCLATH	_	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	er			-000 0000	-000 0000
40Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
40Ch	—	Unimplement	ted							—	_
40Dh	—	Unimplement	ted							_	_
40Eh	_	Unimplement	mplemented							—	
40Fh	_	Unimplement	ted							—	
410h	_	Unimplement	ted							—	
411h	—	Unimplement	ted							_	_
412h	_	Unimplement	ted							—	
413h	—	Unimplement	ted							_	_
414h	—	Unimplement	ted							_	_
415h	TMR4	Timer4 Modu	le Register							0000 0000	0000 0000
416h	PR4	Timer4 Perio	d Register							1111 1111	1111 1111
417h	T4CON	_		T4OUTF	PS<3:0>		TMR4ON	T4CKF	PS<1:0>	-000 0000	-000 0000
418h	—	Unimplement	ted							—	_
419h	—	Unimplement	ted							_	_
41Ah	—	Unimplement	ted							_	_
41Bh	—	Unimplement	ted							_	_
41Ch	TMR6	Timer6 Modu	le Register							0000 0000	0000 0000
41Dh	PR6	Timer6 Perio	d Register							1111 1111	1111 1111
41Eh	T6CON	_		T6OUTF	PS<3:0>		TMR6ON	T6CKF	PS<1:0>	-000 0000	-000 0000
41Fh	—	Unimplement	ted							_	_

TABLE 3-8: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: PIC16F/LF1829 only.

3: PIC16F/LF1825 only.

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Banks 9	9-30										
x00h/ x80h ⁽¹⁾	INDF0	Addressing th (not a physical		es contents of	FSR0H/FSR0)L to address	data memory	,		XXXX XXXX	* **** ****
x00h/ x81h ⁽¹⁾	INDF1	Addressing th (not a physical		es contents of	FSR1H/FSR1	L to address	data memory			XXXX XXXX	* **** ****
x02h/ x82h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant E	3yte					0000 0000	0000 0000
x03h/ x83h ⁽¹⁾	STATUS	—	_	—	TO	PD	Z	DC	С	1 1000	q quuu
x04h/ x84h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poir	nter					0000 0000) uuuu uuuu
x05h/ x85h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Poi	nter					0000 0000	0000 0000
x06h/ x86h ⁽¹⁾	FSR1L	Indirect Data	ect Data Memory Address 1 Low Pointer							0000 0000) uuuu uuuu
x07h/ x87h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Poi	nter					0000 0000	0000 0000
x08h/ x88h ⁽¹⁾	BSR	—	_	—			BSR<4:0>			0 0000	00 0000
x09h/ x89h ⁽¹⁾	WREG	Working Reg	ister							0000 0000) uuuu uuuu
x0Ah/ x8Ah ⁽¹⁾	PCLATH	—	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	er			-000 0000	0 -000 0000
x0Bh/ x8Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0002	0000 000u
x0Ch/ x8Ch	—	Unimplement	ied							-	-
 x1Fh/ x9Fh											

SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED) TABLE 3-8

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: PIC16F/LF1829 only.

3: PIC16F/LF1825 only.

TABLE	3-8: 5	SPECIAL F	UNCTION	REGIST	ER SUMI		JNTINUE	:D)	1		
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 3 ^r	1										
F80h ⁽¹⁾	INDF0	Addressing th (not a physical		es contents of	FSR0H/FSR0)L to address	data memory	/		XXXX XXXX	XXXX XXXX
F81h ⁽¹⁾	INDF1	Addressing th (not a physical		es contents of	FSR1H/FSR1	1L to address	data memory	/		XXXX XXXX	XXXX XXXX
F82h ⁽¹⁾	PCL	Program Cou	inter (PC) Lea	st Significant E	Byte					0000 0000	0000 0000
F83h ⁽¹⁾	STATUS	_	_	_	TO	PD	Z	DC	С	1 1000	q quuu
F84h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poi	nter					0000 0000	uuuu uuuu
F85h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Po	inter					0000 0000	0000 0000
F86h ⁽¹⁾	FSR1L	Indirect Data	Memory Addr	ess 1 Low Poi	nter					0000 0000	uuuu uuuu
F87h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Po	inter					0000 0000	0000 0000
F88h ⁽¹⁾	BSR	_	_	_			BSR<4:0>			0 0000	0 0000
F89h ⁽¹⁾	WREG	Working Reg	ister							0000 0000	uuuu uuuu
F8Ah ⁽¹⁾	PCLATH	_	Write Buffer f	or the upper 7	bits of the Pro	ogram Counte	er			-000 0000	-000 0000
F8Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
F8Ch	—	Unimplement	ed				•	•		_	—
FE3h											
FE4h	STATUS_ SHAD	_	-	-	-	-	Z_SHAD	DC_SHAD	C_SHAD	xxx	uuu
FE5h	WREG_ SHAD	Working Reg	ister Shadow							0000 0000	uuuu uuuu
FE6h	BSR_ SHAD	-	—	—	Bank Select	Register Sha	dow			x xxxx	u uuuu
FE7h	PCLATH	_	Program Cou	Inter Latch Hig	h Register Sh	nadow				-xxx xxxx	uuuu uuuu
	SHAD –										
FE8h	FSR0L_ SHAD	Indirect Data	Memory Addr	ess 0 Low Poi	nter Shadow					XXXX XXXX	uuuu uuuu
FE9h	FSR0H_ SHAD	Indirect Data	Memory Addr	ess 0 High Po	inter Shadow					XXXX XXXX	uuuu uuuu
FEAh	FSR1L_ SHAD	Indirect Data	Memory Addr	ess 1 Low Poi	nter Shadow					XXXX XXXX	uuuu uuuu
FEBh	FSR1H_ SHAD	Indirect Data	Memory Addr	ess 1 High Po	inter Shadow					XXXX XXXX	uuuu uuuu
FECh	_	Unimplement	ed							_	_
FEDh	STKPTR	_	_		Current Stac	k pointer				1 1111	1 1111
FEEh		Top-of-Stack	Low byte							XXXX XXXX	uuuu uuuu
FEFh	TOSL	iop of Oldok	Top-of-Stack	High byte							
	TOSH		тор-от-зласк	i ligit byte						-XXX XXXX	-uuu uuuu

TABLE 3-8 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

 ${\rm x}$ = unknown, ${\rm u}$ = unchanged, ${\rm q}$ = value depends on condition, - = unimplemented, ${\rm r}$ = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: These registers can be addressed from any bank.

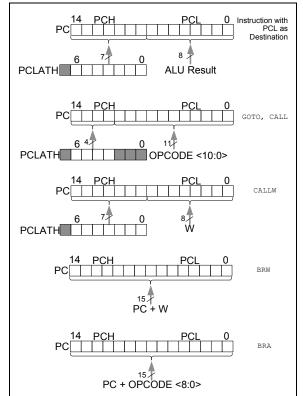
2: PIC16F/LF1829 only.

3: PIC16F/LF1825 only.

3.3 PCL and PCLATH

The Program Counter (PC) is 15 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<14:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 3-3 shows the five situations for the loading of the PC.

FIGURE 3-3: LOADING OF PC IN DIFFERENT SITUATIONS



3.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 7 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

3.3.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note AN556, *"Implementing a Table Read"* (DS00556).

3.3.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

3.3.4 BRANCHING

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 +, the signed value of the operand of the BRA instruction.

3.4 Stack

All devices have a 16-level x 15-bit wide hardware stack (refer to Figures 3-4 through 3-7). The stack space is not part of either program or data space. The PC is PUSHed onto the stack when CALL or CALLW instructions are executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer if the STVREN bit is programmed to '0' (Configuration Word 2). This means that after the stack has been PUSHed sixteen times, the seventeenth PUSH overwrites the value that was stored from the first PUSH. The eighteenth PUSH overwrites the second PUSH (and so on). The STKOVF and STKUNF flag bits will be set on an Overflow/Underflow, regardless of whether the Reset is enabled.

Note 1: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, CALLW, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

3.4.1 ACCESSING THE STACK

The stack is available through the TOSH, TOSL and STKPTR registers. STKPTR is the current value of the Stack Pointer. TOSH:TOSL register pair points to the TOP of the stack. Both registers are read/writable. TOS is split into TOSH and TOSL due to the 15-bit size of the PC. To access the stack, adjust the value of STKPTR, which will position TOSH:TOSL, then read/write to TOSH:TOSL. STKPTR is 5 bits to allow detection of overflow and underflow.

Note:	Care should be taken when modifying the
	STKPTR while interrupts are enabled.

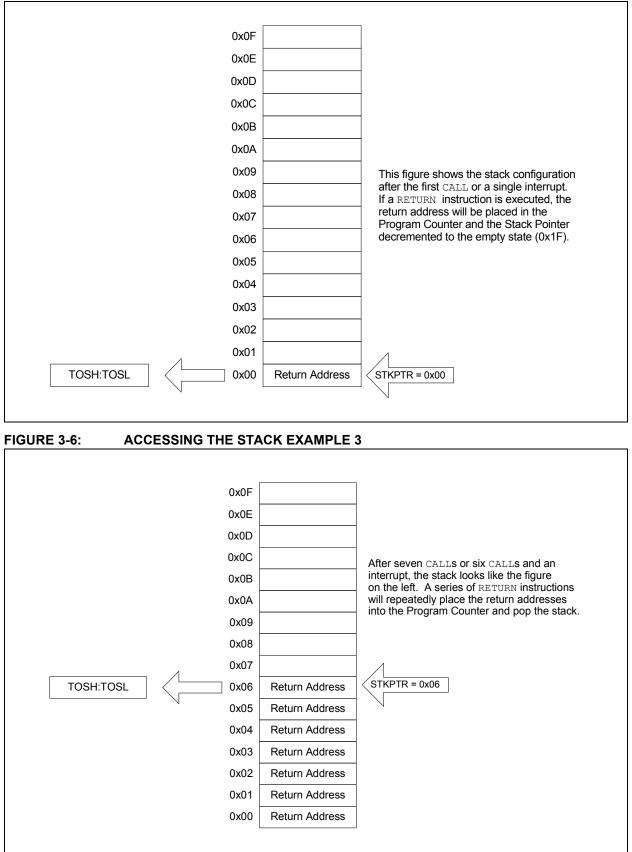
During normal program operation, CALL, CALLW and Interrupts will increment STKPTR while RETLW, RETURN, and RETFIE will decrement STKPTR. At any time STKPTR can be inspected to see how much stack is left. The STKPTR always points at the currently used place on the stack. Therefore, a CALL or CALLW will increment the STKPTR and then write the PC, and a return will unload the PC and then decrement STKPTR.

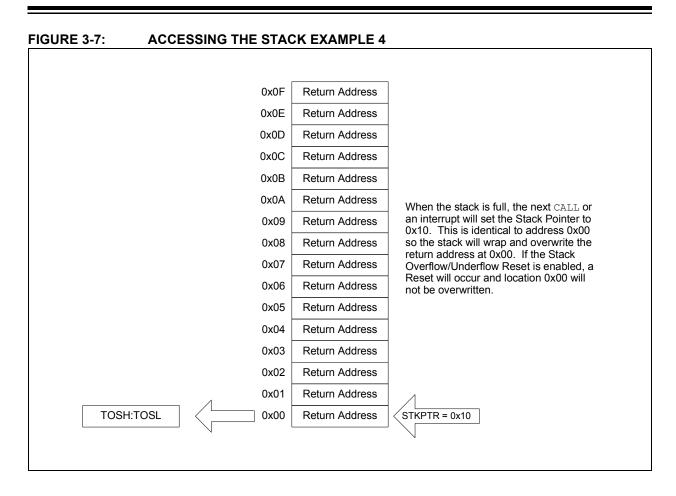
Reference Figure 3-4 through Figure 3-7 for examples of accessing the stack.

FIGURE 3-4: ACCESSING THE STACK EXAMPLE 1

TOSH:TOSL 0x0F	STKPTR = 0x1F Stack Reset Disabled (STVREN = 0)
^N 0х0Е	
0x0D	
0x0C	
0x0B	
0x0A	Initial Stack Configuration:
0×09	
0×08	After Reset, the stack is empty. The empty stack is initialized so the Stack
0x07	Pointer is pointing at 0x1F. If the Stack Overflow/Underflow Reset is enabled, the
0×06	TOSH/TOSL registers will return '0'. If the Stack Overflow/Underflow Reset is
0x05	disabled, the TOSH/TOSL registers will return the contents of stack address 0x0F.
0x04	
0x03	
0x02	
0x01	
0x00	
TOSH:TOSL 0x1F	0x0000 STKPTR = 0x1F Stack Reset Enabled (STVREN = 1)
N	

FIGURE 3-5: ACCESSING THE STACK EXAMPLE 2





3.4.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Word 2 is programmed to '1', the device will be reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

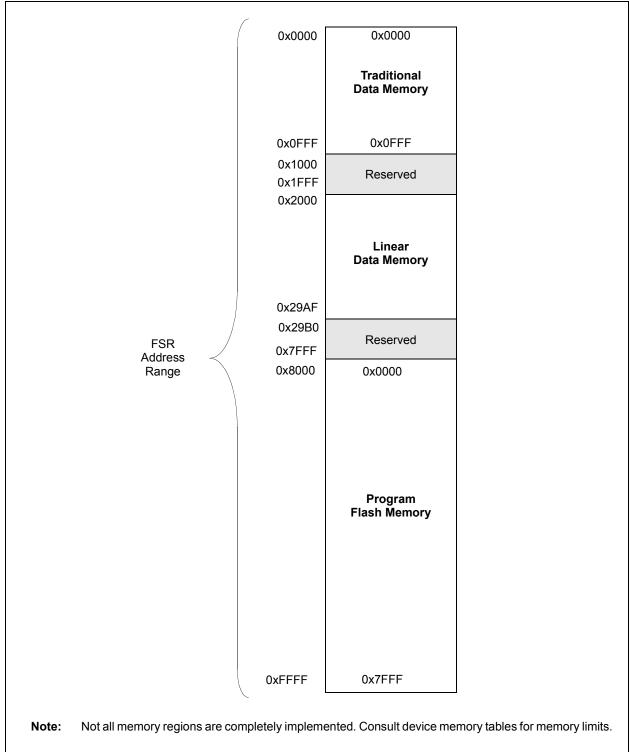
3.5 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional Data Memory
- Linear Data Memory
- Program Flash Memory

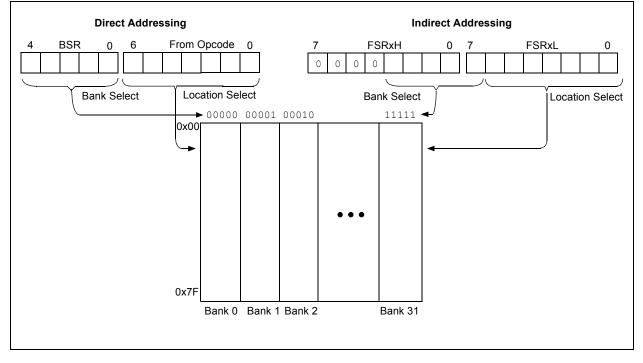
FIGURE 3-8: INDIRECT ADDRESSING



3.5.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address 0x000 to FSR address 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.





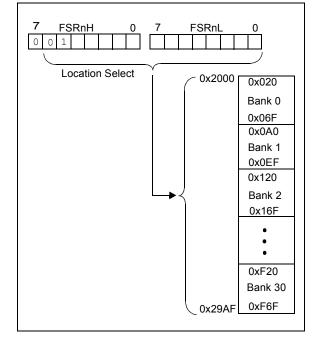
3.5.2 LINEAR DATA MEMORY

The linear data memory is the region from FSR address 0x2000 to FSR address 0x29AF. This region is a virtual region that points back to the 80-byte blocks of GPR memory in all the banks.

Unimplemented memory reads as 0x00. Use of the linear data memory region allows buffers to be larger than 80 bytes because incrementing the FSR beyond one bank will go directly to the GPR memory of the next bank.

The 16 bytes of common memory are not included in the linear data memory region.

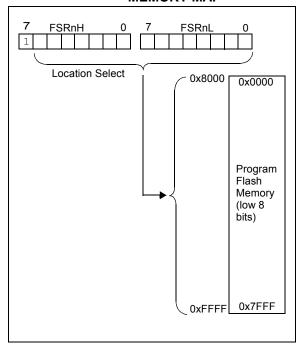
FIGURE 3-10: LINEAR DATA MEMORY MAP



3.5.3 PROGRAM FLASH MEMORY

To make constant data access easier, the entire program Flash memory is mapped to the upper half of the FSR address space. When the MSB of FSRnH is set, the lower 15 bits are the address in program memory which will be accessed through INDF. Only the lower 8 bits of each memory location is accessible via INDF. Writing to the program Flash memory cannot be accomplished via the FSR/INDF interface. All instructions that access program Flash memory via the FSR/INDF interface will require one additional instruction cycle to complete.

FIGURE 3-11: PROGRAM FLASH MEMORY MAP



4.0 DEVICE CONFIGURATION

Device Configuration consists of Configuration Word 1 and Configuration Word 2, Code Protection and Device ID.

4.1 Configuration Words

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as Configuration Word 1 at 8007h and Configuration Word 2 at 8008h.

Note:	The DEBUG bit in Configuration Word 2 is
	managed automatically by device
	development tools including debuggers
	and programmers. For normal device
	operation, this bit should be maintained as
	a '1'.

REGISTER 4-1: CONFIGURATION WORD 1

R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1
FCMEN	IESO	CLKOUTEN	BOREN1	BOREN0	CPD	CP
bit 13	÷	·		·		bit
R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1
MCLRE	PWRTE	WDTE1	WDTE0	FOSC2	FOSC1	FOSC0
bit 6						bit
Legend:						
R = Readable b	vit	W = Writable bit		U = Unimplemente	ed bit. read as '1'	
u = Bit is uncha	nged	x = Bit is unknown	I	•	R and BOR/Value	at all other Reset
'1' = Bit is set	0	'0' = Bit is cleared		P = Programmable		
bit 13	FCMEN: Fail-Sat	fe Clock Monitor Ena	able bit			
		ck Monitor is enable				
bit 12		xternal Switchover b				
51(12		rnal Switchover mod	•			
	0 = Internal/Exte	rnal Switchover mod	e is disabled			
bit 11		ock Out Enable bit				
		ation bits are set to I		<u>s:</u> Dscillator function on	the CLKOUT nin	
	All other FOSC n					
		T function is disable				
		T function is enable		pin		
bit 10-9	BOREN<1:0>: B 11 = BOR enable	rown-out Reset Ena	ble bits(")			
		ed during operation a	and disabled in SI	еер		
	01 = BOR contro	lled by SBOREN bit				
	00 = BOR disable					
bit 8	CPD: Data Code		diaphlad			
		code protection is of code protection protection is of code protection pro				
bit 7	CP: Code Protec					
		mory code protection	n is disabled			
	-	mory code protectior				
bit 6		CLR/VPP Pin Functio	n Select bit			
	<u>If LVP bit = 1</u> : This bit is igr	nored				
	If LVP bit = 0 :					
		PP pin function is \overline{MC}				
	0 = MCLR/V WPUA re		tal input; MCLR int	ernally disabled; Wea	ak pull-up under con	trol of
bit 5		up Timer Enable bit ⁽	1)			
bit 5	1 = PWRT disal					
	0 = PWRT enab	oled				
bit 4-3		tchdog Timer Enabl	e bit			
	11 = WDT enabl		disabled in Slee	n		
		ed while running and olled by the SWDTE		•		
	00 = WDT disab					
			tiaally an abla D			
	abling Brown-out Res		•	ver-up Timer. ction is turned off du	ring an oraco	
			•	otection is turned off	•	

The entire data EEPROM will be erased when the code protection is turned on during
 The entire program memory will be erased when the code protection is turned off.

REGISTER 4-1: CONFIGURATION WORD 1 (CONTINUED)

bit 2-0

FOSC<2:0>: Oscillator Selection bits

- 111 = ECH: External Clock, High-Power mode (4-32 MHz): device clock supplied to CLKIN pin
- 110 = ECM: External Clock, Medium-Power mode (0.5-4 MHz): device clock supplied to CLKIN pin
 - 101 = ECL: External Clock, Low-Power mode (0-0.5 MHz): device clock supplied to CLKIN pin
 - 100 = INTOSC oscillator: I/O function on CLKIN pin
 - 011 = EXTRC oscillator: External RC circuit connected to CLKIN pin
 - 010 = HS oscillator: High-speed crystal/resonator connected between OSC1 and OSC2 pins
 - 001 = XT oscillator: Crystal/resonator connected between OSC1 and OSC2 pins
 - 000 = LP oscillator: Low-power crystal connected between OSC1 and OSC2 pins
- **Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
 - 2: The entire data EEPROM will be erased when the code protection is turned off during an erase.
 - **3:** The entire program memory will be erased when the code protection is turned off.

REGISTER 4-2: CONFIGURATION WORD 2

R/P-1/1	R/P-1/1	U-1	R/P-1/1	R/P-1/1	R/P-1/1	U-1	
LVP	DEBUG ⁽²⁾	—	BORV	STVREN	PLLEN	—	
bit 13		•		· ·		bit	
U-1	U-1	R-1	U-1	U-1	R/P-1/1	R/P-1/1	
	<u> </u>	Reserved			WRT1	WRT0	
bit 6		Rescived			, , , , , , , , , , , , , , , , , , ,	bit	
						2.1	
Legend:							
R = Readable bit		W = Writable bit		U = Unimplemente	ed bit, read as '1'		
u = Bit is unchang	ged	x = Bit is unknown		-n/n = Value at PO	R and BOR/Value	at all other Reset	
'1' = Bit is set		'0' = Bit is cleared		P = Programmable	e bit		
bit 13	1 = Low-voltage	e Programming Ena pro <u>gramm</u> ing enable on MCLR must be u	d	ning			
bit 12	1 = In-Circuit Deb		PCLK and ICSP	DAT are general purp DAT are dedicated to	•		
bit 11	Unimplemented	: Read as '1'					
bit 10	1 = Brown-out Re	It Reset Voltage Sele eset voltage set to 1. eset voltage set to 2.	9V (typical)				
bit 9	1 = Stack Overflo	Overflow/Underflow ow or Underflow will ow or Underflow will	cause a Reset				
bit 8	PLLEN: PLL Ena 1 = 4xPLL enable 0 = 4xPLL disable	ed					
bit 7-5	Unimplemented	: Read as '1'					
bit 4	Reserved: This I	ocation should be pr	ogrammed to a '	1'.			
	Unimplemented	: Read as '1'					
bit 3-2	 WRT<1:0>: Flash Memory Self-Write Protection bits 11 = Write protection off 10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by EECON control 01 = 000h to 3FFh write-protected, 400h to 7FFh may be modified by EECON control 00 = 000h to 7FFh write-protected, no addresses may be modified by EECON control 						

2: The DEBUG bit in Configuration Word is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.

4.2 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data EEPROM protection are controlled independently. Internal access to the program memory and data EEPROM are unaffected by any code protection setting.

4.2.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the \overline{CP} bit in Configuration Word 1. When $\overline{CP} = 0$, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See Section 4.3 "Write Protection" for more information.

4.2.2 DATA EEPROM PROTECTION

The entire data EEPROM is protected from external reads and writes by the CPD bit. When $\overline{CPD} = 0$, external reads and writes of data EEPROM are inhibited. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

4.3 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Word 2 define the size of the program memory block that is protected.

4.4 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See Section 11.5 "User ID, Device ID and Configuration Word Access" for more information on accessing these memory locations. For more information on checksum calculation, see the "*PIC16F/LF182X/PIC12F/LF1822 Memory Programming Specification*" (DS41390).

4.5 Device ID and Revision ID

The memory location 8006h is where the Device ID and Revision ID are stored. The upper nine bits hold the Device ID. The lower five bits hold the Revision ID. See Section 11.5 "User ID, Device ID and Configuration Word Access" for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

REGISTER 4-3: DEVICEID: DEVICE ID REGISTER⁽¹⁾

R	R	R	R	R	R	R		
DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2		
bit 13						bit 7		
R	R	R	R	R	R	R		
DEV1	DEV0	REV4	REV3	REV2	REV1	REV0		
bit 6						bit 0		
Legend:				U = Unimplemented bit, read as '0'				
R = Readable bit W = Writable bit			'0' = Bit is cleared					
-n = Value at POF	-n = Value at POR '1' = Bit is set			x = Bit is unknown				
bit 13-5	DEV<8:0>: Device ID bits 100111011 = PIC16F1825 100111111 = PIC16F1829							
	100111111 = PIC16LF1825 101000111 = PIC16LF1825 101000111 = PIC16LF1829							
bit 4-0	REV<4:0>: Revision ID bits							
	These bits are used to identify the revision.							

Note 1: This location cannot be written.

5.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

5.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 5-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability
 of crystal oscillator sources

The oscillator module can be configured in one of eight clock modes.

- 1. ECL External Clock Low Power mode (0 MHz to 0.5 MHz)
- 2. ECM External Clock Medium Power mode (0.5 MHz to 4 MHz)
- 3. ECH External Clock High Power mode (4 MHz to 32 MHz)
- 4. LP 32 kHz Low-Power Crystal mode.
- 5. XT Medium Gain Crystal or Ceramic Resonator Oscillator mode (up to 4 MHz)
- 6. HS High Gain Crystal or Ceramic Resonator mode (4 MHz to 20 MHz)
- 7. RC External Resistor-Capacitor (RC).
- 8. INTOSC Internal oscillator (31 kHz to 32 MHz).

Clock Source modes are selected by the FOSC<2:0> bits in the Configuration Word 1. The FOSC bits determine the type of oscillator that will be used when the device is first powered.

The EC clock mode relies on an external logic level signal as the device clock source. The LP, XT and HS clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The RC clock mode requires an external resistor and capacitor to set the oscillator frequency.

The INTOSC internal oscillator block produces low, medium, and high frequency clock sources, designated LFINTOSC, MFINTOSC, and HFINTOSC. (see Internal Oscillator Block, Figure 5-1). A wide selection of device clock frequencies may be derived from these three clock sources.

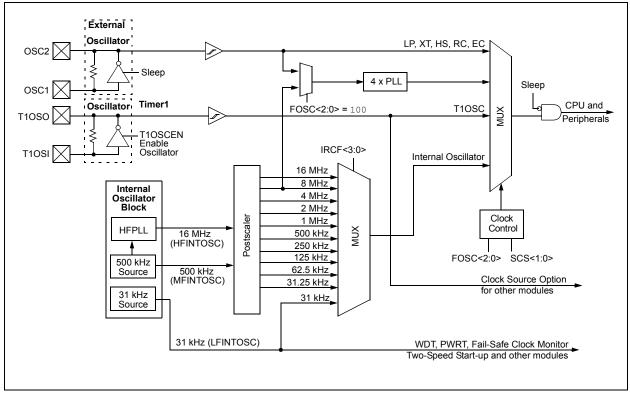


FIGURE 5-1: SIMPLIFIED PIC[®] MCU CLOCK SOURCE BLOCK DIAGRAM

5.2 Clock Source Types

Clock sources can be classified as external or internal.

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.

Internal clock sources are contained internally within the oscillator module. The internal oscillator block has two internal oscillators and a dedicated phase-locked loop (HFPLL) that are used to generate three internal system clock sources: the 16 MHz High-Frequency Internal Oscillator (HFINTOSC), 500 kHZ (MFINTOSC) and the 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS) bits in the OSCCON register. See Section 5.3 "Clock Switching" for additional information.

5.2.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in the Configuration Word 1 to select an external clock source that will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to:
 - Timer1 Oscillator during run-time, or
 - An external clock source determined by the value of the FOSC bits.

See Section 5.3 "Clock Switching" for more information.

5.2.1.1 EC Mode

The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 5-2 shows the pin connections for EC mode.

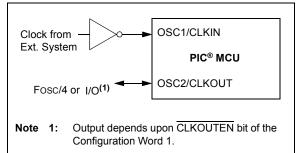
EC mode has 3 power modes to select from through Configuration Word 1:

- High-power, 4-32 MHz (FOSC = 111)
- Medium power, 0.5-4 MHz (FOSC = 110)
- Low-power, 0-0.5 MHz (FOSC = 101)

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC[®] MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 5-2:

EXTERNAL CLOCK (EC) MODE OPERATION



5.2.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 5-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

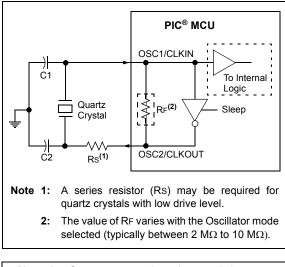
XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 5-3 and Figure 5-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 5-3:

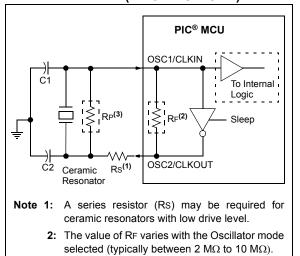
QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



- Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
 - 2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.
 - **3:** For oscillator design assistance, reference the following Microchip Application Notes:
 - AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC[®] and PIC[®] Devices" (DS00826)
 - AN849, "Basic PIC[®] Oscillator Design" (DS00849)
 - AN943, "Practical PIC[®] Oscillator Analysis and Design" (DS00943)
 - AN949, "Making Your Oscillator Work" (DS00949)

FIGURE 5-4: CERAMIC RESONATOR

OPERATION (XT OR HS MODE)



3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

5.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see Section 5.4 "Two-Speed Clock Start-up Mode").

5.2.1.4 4X PLL

The oscillator module contains a 4X PLL that can be used with both external and internal clock sources to provide a system clock source. The input frequency for the 4X PLL must fall within specifications. See the PLL Clock Timing Specifications in **Section 30.0 "Electrical Specifications"**.

The 4X PLL may be enabled for use by one of two methods:

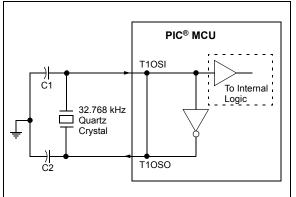
- 1. Program the PLLEN bit in Configuration Word 2 to a '1'.
- Write the SPLLEN bit in the OSCCON register to a '1'. If the PLLEN bit in Configuration Word 2 is programmed to a '1', then the value of SPLLEN is ignored.

5.2.1.5 TIMER1 Oscillator

The Timer1 Oscillator is a separate crystal oscillator that is associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the T1OSO and T1OSI device pins.

The Timer1 Oscillator can be used as an alternate system clock source and can be selected during run-time using clock switching. Refer to **Section 5.3 "Clock Switching**" for more information.

FIGURE 5-5: QUARTZ CRYSTAL OPERATION (TIMER1 OSCILLATOR)



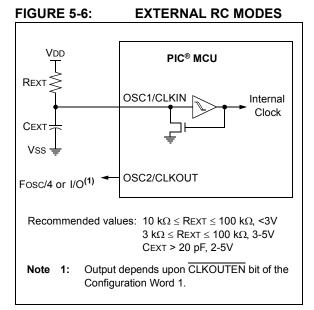
- Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
 - 2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.
 - **3:** For oscillator design assistance, reference the following Microchip Application Notes:
 - AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC[®] and PIC[®] Devices" (DS00826)
 - AN849, "Basic PIC[®] Oscillator Design" (DS00849)
 - AN943, "Practical PIC[®] Oscillator Analysis and Design" (DS00943)
 - AN949, "Making Your Oscillator Work" (DS00949)
 - TB097, "Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS" (DS91097)
 - AN1288, "Design Practices for Low-Power External Oscillators" (DS01288)

5.2.1.6 External RC Mode

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required.

The RC circuit connects to OSC1. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. The function of the OSC2/CLKOUT pin is determined by the state of the CLKOUTEN bit in Configuration Word 1.

Figure 5-6 shows the external RC mode connections.



The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- · packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

5.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in Configuration Word 1 to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to the internal oscillator during run-time. See Section 5.3 "Clock Switching"for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the state of the $\overline{\text{CLKOUTEN}}$ bit in Configuration Word 1.

The internal oscillator block has two independent oscillators and a dedicated Phase-Locked Loop, HFPLL that can produce one of three internal system clock sources.

- The HFINTOSC (High-Frequency Internal Oscillator) is factory calibrated and operates at 16 MHz. The HFINTOSC source is generated from the 500 kHz MFINTOSC source and the dedicated Phase-Locked Loop, HFPLL. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
- The MFINTOSC (Medium-Frequency Internal Oscillator) is factory calibrated and operates at 500 kHz. The frequency of the MFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
- 3. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

5.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 5-3).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). One of nine frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See Section 5.2.2.7 "Internal Oscillator Clock Switch Timing" for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'.

The High Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running and can be utilized.

The High Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High Frequency Internal Oscillator Status Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

5.2.2.2 MFINTOSC

The Medium-Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register (Register 5-3).

The output of the MFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See Section 5.2.2.7 "Internal Oscillator Clock Switch Timing" for more information.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

The Medium Frequency Internal Oscillator Ready bit (MFIOFR) of the OSCSTAT register indicates when the MFINTOSC is running and can be utilized.

5.2.2.3 Internal Oscillator Frequency Adjustment

The 500 kHz internal oscillator is factory calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 5-3). Since the HFINTOSC and MFINTOSC clock sources are derived from the 500 kHz internal oscillator a change in the OSCTUNE register value will apply to both.

The default value of the OSCTUNE register is '0'. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

5.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). Select 31 kHz, via software, using the IRCF<3:0> bits of the OSCCON register. See Section 5.2.2.7 "Internal Oscillator Clock Switch Timing" for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<3:0> bits of the OSCCON register = 000) as the system clock source (SCS bits of the OSCCON register = 1x), or when any of the following are enabled:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired LF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

Peripherals that use the LFINTOSC are:

- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The Low Frequency Internal Oscillator Ready bit (LFIOFR) of the OSCSTAT register indicates when the LFINTOSC is running and can be utilized.

5.2.2.5 Internal Oscillator Frequency Selection

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register.

The output of the 16 MHz HFINTOSC and 31 kHz LFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). The Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register select the frequency output of the internal oscillators. One of the following frequencies can be selected via software:

- 32 MHz (requires 4X PLL)
- 16 MHz
- 8 MHz
- 4 MHz
- 2 MHz
- 1 MHz
- 500 kHz (Default after Reset)
- 250 kHz
- 125 kHz
- 62.5 kHz
- 31.25 kHz
- 31 kHz (LFINTOSC)

Note:	Following any Reset, the IRCF<3:0> bits
	of the OSCCON register are set to '0111'
	and the frequency selection is set to
	500 kHz. The user can modify the IRCF
	bits to select a different frequency.

The IRCF<3:0> bits of the OSCCON register allow duplicate selections for some frequencies. These duplicate choices can offer system design trade-offs. Lower power consumption can be obtained when changing oscillator sources for a given frequency. Faster transition times can be obtained between frequency changes that use the same oscillator source.

5.2.2.6 32 MHz Internal Oscillator Frequency Selection

The Internal Oscillator Block can be used with the 4X PLL associated with the External Oscillator Block to produce a 32 MHz internal system clock source. The following settings are required to use the 32 MHz internal clock source:

- The FOSC bits in Configuration Word 1 must be set to use the INTOSC source as the device system clock (FOSC<2:0> = 100).
- The SCS bits in the OSCCON register must be cleared to use the clock determined by FOSC<2:0> in Configuration Word 1 (SCS<1:0> = 00).
- The IRCF bits in the OSCCON register must be set to the 8 MHz HFINTOSC set to use (IRCF<3:0> = 1110).
- The SPLLEN bit in the OSCCON register must be set to enable the 4xPLL, or the PLLEN bit of the Configuration Word 2 must be programmed to a '1'.
- Note: When using the PLLEN bit of the Configuration Word 2, the 4xPLL cannot be disabled by software and the 8 MHz HFINTOSC option will no longer be available.

The 4xPLL is not available for use with the internal oscillator when the SCS bits of the OSCCON register are set to '1x'. The SCS bits must be set to '00' to use the 4xPLL with the internal oscillator.

5.2.2.7 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC, MFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 5-7). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC, MFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

- 1. IRCF<3:0> bits of the OSCCON register are modified.
- 2. If the new clock is shut down, a clock start-up delay is started.
- 3. Clock switch circuitry waits for a falling edge of the current clock.
- 4. The current clock is held low and the clock switch circuitry waits for a rising edge in the new clock.
- 5. The new clock is now active.
- 6. The OSCSTAT register is updated as required.
- 7. Clock switch is complete.

See Figure 5-7 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected. Clock switching time delays are shown in Table 5-1.

Start-up delay specifications are located in the oscillator tables of Section 30.0 "Electrical Specifications"

FIGURE 5-7:	INTERNAL OSCILLATOR SWITCH TIMING
MFINTOSC HFINTOSC/	LFINTOSC (FSCM and WDT disabled)
MFINTOSC LFINTOSC	Start-up Time 2-cycle Sync Running
IRCF <3:0>	
System Clock HFINTOSC/→ MFINTOSC	LFINTOSC (Either FSCM or WDT enabled)
HFINTOSC/ MFINTOSC	
LFINTOSC	
IRCF <3:0>	$\neq 0$ $X = 0$
System Clock	
LFINTOSC →	HFINTOSC/MFINTOSC LFINTOSC turns off unless WDT or FSCM is enabled
LFINTOSC	Start-up Time 2-cycle Sync Running
HFINTOSC/ MFINTOSC	
IRCF <3:0>	$= 0 \qquad \chi \qquad \neq 0$
System Clock	

5.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS bits:

- Default system oscillator determined by FOSC bits in Configuration Word 1
- Timer1 32 kHz crystal oscillator
- Internal Oscillator Block (INTOSC)

5.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS) bits of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bits of the OSCCON register = 00, the system clock source is determined by value of the FOSC<2:0> bits in the Configuration Word 1.
- When the SCS bits of the OSCCON register = 01, the system clock source is the Timer1 oscillator.
- When the SCS bits of the OSCCON register = 1x, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0> bits of the OSCCON register. After a Reset, the SCS bits of the OSCCON register are always cleared.

Note:	Any automatic clock switch, which may								
	occur from Two-Speed Start-up or								
	Fail-Safe Clock Monitor, does not update								
	the SCS bits of the OSCCON register. The								
	user can monitor the OSTS bit of the								
	OSCSTAT register to determine the current								
	system clock source.								

When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 5-1.

5.3.2 OSCILLATOR START-UP TIME-OUT STATUS (OSTS) BIT

The Oscillator Start-up Time-out Status (OSTS) bit of the OSCSTAT register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word 1, or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes. The OST does not reflect the status of the Timer1 Oscillator.

5.3.3 TIMER1 OSCILLATOR

The Timer1 Oscillator is a separate crystal oscillator associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the T1OSO and T1OSI device pins.

The Timer1 oscillator is enabled using the T1OSCEN control bit in the T1CON register. See Section 21.0 "Timer1 Module with Gate Control" for more information about the Timer1 peripheral.

5.3.4 TIMER1 OSCILLATOR READY (T1OSCR) BIT

The user must ensure that the Timer1 Oscillator is ready to be used before it is selected as a system clock source. The Timer1 Oscillator Ready (T1OSCR) bit of the OSCSTAT register indicates whether the Timer1 oscillator is ready to be used. After the T1OSCR bit is set, the SCS bits can be configured to select the Timer1 oscillator.

5.4 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC internal oscillator block as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for LP, XT or HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the OSTS bit of the OSCSTAT register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

Note:	Executing a SLEEP instruction will abort					
	the oscillator start-up time and will cause					
	the OSTS bit of the OSCSTAT register to					
	remain clear.					

5.4.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Word 1) = 1; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = 00.
- FOSC<2:0> bits in the Configuration Word 1 configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

Switch From	Switch To	Frequency	Oscillator Delay		
Sleep/POR	LFINTOSC ⁽¹⁾ MFINTOSC ⁽¹⁾ HFINTOSC ⁽¹⁾	MFINTOSC ⁽¹⁾ 31.25 kHz-500 kHz Oscillator Warm-up HFINTOSC ⁽¹⁾ 31.25 kHz-16 MHz			
Sleep/POR	EC, RC ⁽¹⁾	DC – 32 MHz	2 cycles		
LFINTOSC	EC, RC ⁽¹⁾	DC – 32 MHz	1 cycle of each		
Sleep/POR	Timer1 Oscillator LP, XT, HS ⁽¹⁾	32 kHz-20 MHz	1024 Clock Cycles (OST)		
Any clock source	MFINTOSC ⁽¹⁾ HFINTOSC ⁽¹⁾	31.25 kHz-500 kHz 31.25 kHz-16 MHz	2 μs (approx.)		
Any clock source	LFINTOSC ⁽¹⁾	31 kHz	1 cycle of each		
Any clock source	Timer1 Oscillator	32 kHz	1024 Clock Cycles (OST)		
PLL inactive	PLL inactive PLL active 16-32 MHz 2 ms (approx.)		2 ms (approx.)		

Note 1: PLL inactive.

5.4.2 TWO-SPEED START-UP SEQUENCE

- 1. Wake-up from Power-on Reset or Sleep.
- 2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF<3:0> bits of the OSCCON register.
- 3. OST enabled to count 1024 clock cycles.
- 4. OST timed out, wait for falling edge of the internal oscillator.
- 5. OSTS is set.
- 6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
- 7. System clock is switched to external clock source.

5.4.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCSTAT register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word 1, or the internal oscillator.

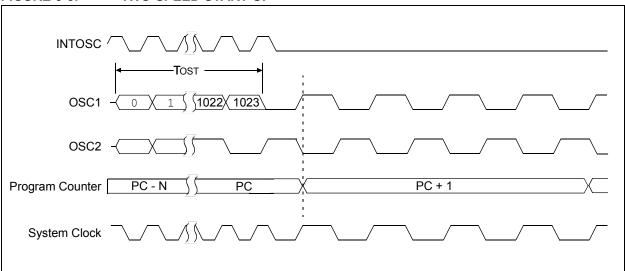
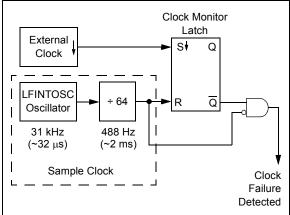


FIGURE 5-8: TWO-SPEED START-UP

5.5 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Word 1. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, EC, Timer1 Oscillator and RC).

FIGURE 5-9: FSCM BLOCK DIAGRAM



5.5.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 5-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

5.5.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR2 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE2 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<3:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

5.5.3 FAIL-SAFE CONDITION CLEARING

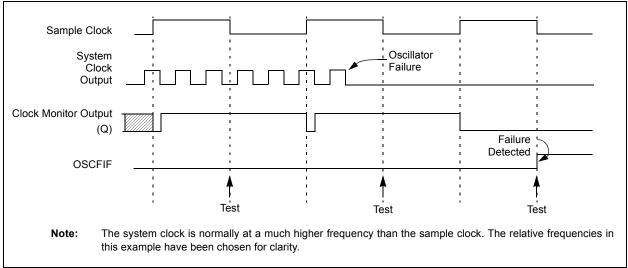
The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the SCS bits of the OSCCON register. When the SCS bits are changed, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared and the device will be operating from the external clock source. The Fail-Safe condition must be cleared before the OSFIF flag can be cleared.

5.5.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note: Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the Status bits in the OSCSTAT register to verify the oscillator start-up and that the system clock switchover has successfully completed.





5.6 Oscillator Control Registers

R/W-0/0	R/W-0/0	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-0/0	R/W-0/0			
SPLLEN		IRCF	<3:0>			SCS	<1:0>			
bit 7							bit			
Legend:										
R = Readabl	e bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'				
u = Bit is und	hanged	x = Bit is unkr	nown	-		DR/Value at all	other Resets			
'1' = Bit is se	-	'0' = Bit is cle								
bit 7	SPLLEN: So	oftware PLL Ena	able bit							
		If PLLEN in Configuration Word 1 = 1:								
	SPLLEN bit	SPLLEN bit is ignored. 4x PLL is always enabled (subject to oscillator requirements)								
		If PLLEN in Configuration Word 1 = 0:								
		1 = 4x PLL ls enabled 0 = 4x PLL is disabled								
			_	.						
bit 6-3		Internal Oscillat	or Frequency	Select bits						
	000x = 31 k 0010 = 31.2									
	0010 = 31.2									
	0100 = 62.5									
	0101 = 125									
	0110 = 250 kHz MF									
	0111 = 500 kHz MF (default upon Reset) 1000 = 125 kHz HF ⁽¹⁾									
	1001 = 250 kHz HF ⁽¹⁾ 1010 = 500 kHz HF ⁽¹⁾									
		1011 = 1 MHz HF								
	1100 = 2 M	Hz HF								
		1101 = 4 MHz HF								
	1110 = 8 MHz or 32 MHz HF(see Section 5.2.2.1 "HFINTOSC") 1111 = 16 MHz HF									
bit 2		nted: Read as '	0'							
	-									
bit 1-0		System Clock S								
	1x = Interna 01 = Timer1									
		00 = Clock determined by FOSC<2:0> in Configuration Word 1.								
loto to D										

REGISTER 5-1: OSCCON: OSCILLATOR CONTROL REGISTER

Note 1: Duplicate frequency derived from HFINTOSC.

R-1/q	R-0/q	R-q/q	R-0/q	R-0/q	R-q/q	R-0/0	R-0/q				
T10SCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS				
bit 7							bit C				
Legend:	- 1-14		L :1			L = = (O)					
R = Readable		W = Writable		•	nented bit, read		athar Daaata				
u = Bit is unc '1' = Bit is se	0	x = Bit is unk			at POR and BO	R/Value at all o	olner Resels				
I = DILIS SE		'0' = Bit is cle	areu	q = Condition	al						
bit 7	T10SCR: T	ïmer1 Oscillator	Ready bit								
	If T10SCEN		rioudy sit								
		oscillator is rea	ıdy								
	0 = Timer1	oscillator is not	ready								
		<u>If T10SCEN = 0</u> :									
		clock source is	always ready								
bit 6		L Ready bit									
	1 = 4x PLL is ready 0 = 4x PLL is not ready										
bit 5		OSTS: Oscillator Start-up Time-out Status bit									
	1 = Running from the clock defined by the FOSC<2:0> bits of the Configuration Word 1										
	0 = Runnir	0 = Running from an internal oscillator (FOSC<2:0> = 100)									
bit 4	HFIOFR: High Frequency Internal Oscillator Ready bit										
	1 = HFINTOSC is ready										
	0 = HFINTOSC is not ready										
bit 3	HFIOFL: High Frequency Internal Oscillator Locked bit										
	 1 = HFINTOSC is at least 2% accurate 0 = HFINTOSC is not 2% accurate 										
bit 2		edium Frequen		illator Ready bi	i+						
		OSC is ready		mator ready b	it.						
		OSC is not read	у								
bit 1	LFIOFR: Low Frequency Internal Oscillator Ready bit										
	1 = LFINTOSC is ready										
	0 = LFINTC	OSC is not ready	/								
bit 0		gh Frequency Ir		or Stable bit							
	 1 = HFINTOSC is at least 0.5% accurate 0 = HFINTOSC is not 0.5% accurate 										
	0 = HFINT(USC is not 0.5%	accurate								

REGISTER 5-2: OSCSTAT: OSCILLATOR STATUS REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0			
_				TUN	<5:0>					
bit 7							bit 0			
Legend:										
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'				
u = Bit is unc	hanged	x = Bit is unkr	known -n/n = Value at POR and BOR/Value at all other Rese							
'1' = Bit is set '0' = Bit is cleared										
bit 7-6	Unimpleme	nted: Read as '	0'							
bit 5-0	TUN<5:0>:	Frequency Tunir	ng bits							
		Aaximum freque	ncy							
	011110 =									
	•									
	•									
	000001 =	000001 =								
		Oscillator module	e is running at	the factory-calil	prated frequen	cy.				
	111111 =									
	•									
	•									

REGISTER 5-3: OSCTUNE: OSCILLATOR TUNING REGISTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page	
OSCCON	SPLLEN		IRCF	IRCF<3:0> —				SCS<1:0>		
OSCSTAT	T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	72	
OSCTUNE	_	_			TUN	<5:0>			73	
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	95	
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	99	
T1CON	TMR1C	S<1:0>	T1CKP	S<1:0>	T10SCEN	T1SYNC	_	TMR10N	199	

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

TABLE 5-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
	13:8		_	FCMEN	IESO	CLKOUTEN	BOREI	N<1:0>	CPD	50
CONFIG1	7:0	CP	MCLRE	PWRTE	WDTE	E<1:0>		FOSC<2:0>		52

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

Note 1: PIC16F1825/1829 only.

NOTES:

6.0 REFERENCE CLOCK MODULE

The reference clock module provides the ability to send a divided clock to the clock output pin of the device (CLKR) and provide a secondary internal clock source to the modulator module. This module is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application. The reference clock module includes the following features:

- System clock is the source
- Available in all oscillator configurations
- · Programmable clock divider
- Output enable to a port pin
- · Selectable duty cycle
- Slew rate control

The reference clock module is controlled by the CLKRCON register (Register 6-1) and is enabled when setting the CLKREN bit. To output the divided clock signal to the CLKR port pin, the CLKROE bit must be set. The CLKRDIV<2:0> bits enable the selection of 8 different clock divider options. The CLKRDC<1:0> bits can be used to modify the duty cycle of the output clock⁽¹⁾. The CLKRSLR bit controls slew rate limiting.

Note 1: If the base clock rate is selected without a divider, the output clock will always have a duty cycle equal to that of the source clock, unless a 0% duty cycle is selected. If the clock divider is set to base clock/2, then 25% and 75% duty cycle accuracy will be dependent upon the source clock.

For information on using the reference clock output with the modulator module, see **Section 23.0 "Data Signal Modulator**".

6.1 Slew Rate

The slew rate limitation on the output port pin can be disabled. The slew rate limitation can be removed by clearing the CLKRSLR bit in the CLKRCON register.

6.2 Effects of a Reset

Upon any device Reset, the reference clock module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

6.3 Conflicts with the CLKR Pin

There are two cases when the reference clock output signal cannot be output to the CLKR pin, if:

- LP, XT or HS Oscillator mode is selected.
- CLKOUT function is enabled.

Even if either of these cases are true, the module can still be enabled and the reference clock signal may be used in conjunction with the modulator module.

6.3.1 OSCILLATOR MODES

If LP, XT or HS oscillator modes are selected, the OSC2/CLKR pin must be used as an oscillator input pin and the CLKR output cannot be enabled. See **Section 5.2 "Clock Source Types"** for more information on different oscillator modes.

6.3.2 CLKOUT FUNCTION

The CLKOUT function has a higher priority than the reference clock module. <u>Therefore, if</u> the CLKOUT function is enabled by the CLKOUTEN bit in Configuration Word 1, Fosc/4 will always be output on the port pin. Reference **Section 4.0** "**Device Configuration**" for more information.

6.4 Operation During Sleep

As the reference clock module relies on the system clock as its source, and the system clock is disabled in Sleep, the module does not function in Sleep, even if an external clock source or the Timer1 clock source is configured as the system clock. The module outputs will remain in their current state until the device exits Sleep.

	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
CLKREN	CLKROE	CLKRSLR	CLKRDC1	CLKRDC0	CLKRDIV2	CLKRDIV1	CLKRDIV0	
pit 7							bit (
_egend:								
R = Readable		W = Writable		•	nented bit, read			
u = Bit is uncha	anged	x = Bit is unkr		-n/n = Value a	at POR and BO	R/Value at all	other Resets	
1' = Bit is set		'0' = Bit is clea	ared					
oit 7	CLKREN: Re	ference Clock	Module Enable	e bit				
		e Clock modul Clock modul						
bit 6	CLKROE: Reference Clock Output Enable bit ⁽³⁾ 1 = Reference Clock output is enabled on CLKR pin							
pit 5		= Reference Clock output disabled on CLKR pin						
JIL O	1 = Slew Rat	.KRSLR: Reference Clock Slew Rate Control Limiting Enable bit Slew Rate limiting is enabled Slew Rate limiting is disabled						
oit 4-3	CLKRDC<1:0	0>: Reference	Clock Duty Cy	cle bits				
	10 = Clock o 01 = Clock o	utputs duty cyc utputs duty cyc utputs duty cyc utputs duty cyc	le of 50% le of 25%					
oit 2-0	CLKRDIV<2:	0> Reference	Clock Divider b	oits				
	110 = Base (101 = Base (100 = Base (011 = Base (010 = Base (clock value divi clock value divi clock value divi clock value divi clock value divi clock value divi clock value divi	ded by 64 ded by 32 ded by 16 ded by 8 ded by 4					

REGISTER 6-1: CLKRCON: REFERENCE CLOCK CONTROL REGISTER

is selected.
3: To route CLKR to pin, CLKOUTEN of Configuration Word 1 = 1 is required. CLKOUTEN of Configuration Word 1 = 0 will result in Fosc/4. See Section 6.3 "Conflicts with the CLKR Pin" for details.

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH REFERENCE CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CLKRCON	CLKREN	CLKROE	CLKRSLR	CLKRDC1	CLKRDC0	CLKRDIV2	CLKRDIV1	CLKRDIV0	76
Legend: -	Legend: — = unimplemented locations read as '0'. Shaded cells are not used by reference clock sources.								

Legend: — = unimplemented locations read as '0'. Shaded cells are not used by reference clock sources.

TABLE 6-2: SUMMARY OF CONFIGURATION WORD WITH REFERENCE CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	_	_	FCMEN	IESO	CLKOUTEN	BOREN1	BOREN0	CPD	50
CONFIGI	7:0	CP	MCLRE	PWRTE	WDTE1	WDTE0	FOSC2	FOSC1	FOSC0	52

Legend: — = unimplemented locations read as '0'. Shaded cells are not used by reference clock sources.

NOTES:

7.0 RESETS

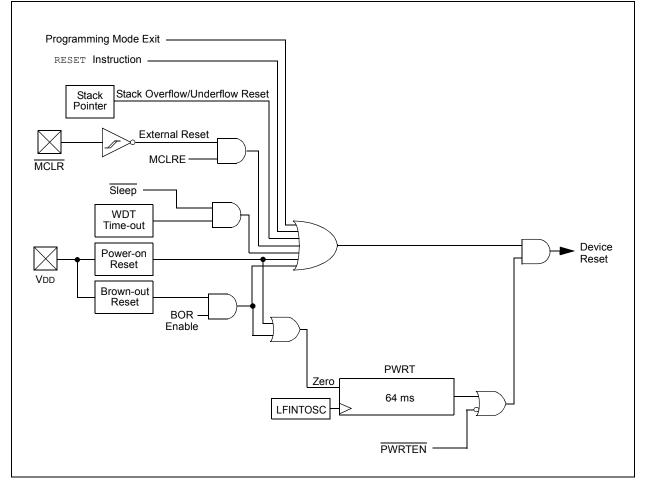
There are multiple ways to reset this device:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- MCLR Reset
- WDT Reset
- RESET instruction
- · Stack Overflow
- Stack Underflow
- Programming mode exit

To allow VDD to stabilize, an optional power-up timer can be enabled to extend the Reset time after a BOR or POR event.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 7-1.

FIGURE 7-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



7.1 Power-on Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

7.1.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a nominal 64 ms timeout on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the PWRTE bit in Configuration Word 1.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00607).

7.2 Brown-Out Reset (BOR)

The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Word 1. The four operating modes are:

- · BOR is always on
- · BOR is off when in Sleep
- · BOR is controlled by software
- · BOR is always off

Refer to Table 7-3 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV bit in Configuration Word 2.

A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below VBOR for a duration greater than parameter TBORDC, the device will reset. See Figure 7-3 for more information.

BOREN Config bits	SBOREN	Device Mode	BOR Mode	Device Operation upon release of POR	Device Operation upon wake- up from Sleep
BOR_ON (11)	Х	Х	Active	Waits for BOR ready ⁽¹⁾	
BOR_NSLEEP (10)	Х	Awake	Active		
BOR_NSLEEP (10)	Х	Sleep	Disabled	- Waits for BOR ready	
BOR_SBOREN (01)	1	X	Active	Begins immediately	
BOR_SBOREN (01)	0	Х	Disabled	Begins immediately	
BOR_OFF (00)	X	X	Disabled	Begins im	mediately

TABLE 7-1:BOR OPERATING MODES

Note 1: Even though this case specifically waits for the BOR, the BOR is already operating, so there is no delay in start-up.

7.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Word 1 are set to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

7.2.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Word 1 are set to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

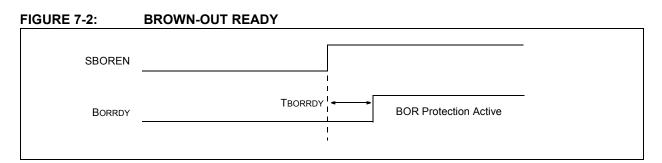
7.2.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Word 1 are set to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

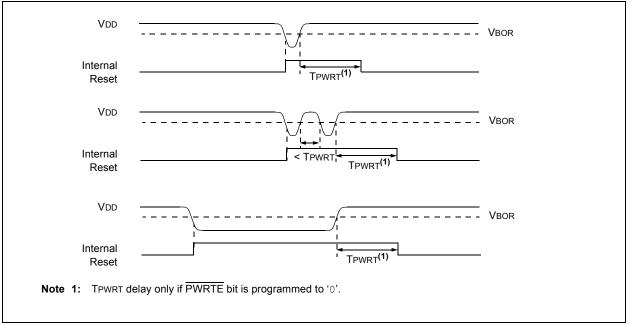
BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

PIC16F/LF1825/1829







REGISTER 7-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	U-0	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN	—	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7	SBOREN: Software Brown-out Reset Enable bit If BOREN <1:0> in Configuration Word $1 \neq 01$: SBOREN is read/write, but has no effect on the BOR. If BOREN <1:0> in Configuration Word 1 = 01:
	1 = BOR Enabled 0 = BOR Disabled
bit 6-1	Unimplemented: Read as '0'
bit 0	BORRDY: Brown-out Reset Circuit Ready Status bit 1 = The Brown-out Reset circuit is active 0 = The Brown-out Reset circuit is inactive

7.3 MCLR

The $\overline{\text{MCLR}}$ is an optional external input that can reset the device. The $\overline{\text{MCLR}}$ function is controlled by the MCLRE bit of Configuration Word 1 and the LVP bit of Configuration Word 2 (Table 7-2).

MCLRE	LVP	MCLR
0	0	Disabled
1	0	Enabled
х	1	Enabled

7.3.1 MCLR ENABLED

When MCLR is enabled and the pin is held low, the device is held in Reset. The MCLR pin is connected to VDD through an internal weak pull-up.

The device has a noise filter in the $\overline{\text{MCLR}}$ Reset path. The filter will detect and ignore small pulses.

Note: A Reset does not drive the MCLR pin low.

7.3.2 MCLR DISABLED

When MCLR is disabled, the pin functions as a general purpose input and the internal weak pull-up is under software control. See Section 12.2 "PORTA Registers" for more information.

7.4 Watchdog Timer (WDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The \overline{TO} and \overline{PD} bits in the STATUS register are changed to indicate the WDT Reset. See Section 10.0 "Watchdog Timer" for more information.

7.5 RESET Instruction

A RESET instruction will cause a device Reset. The \overline{RI} bit in the PCON register will be set to '0'. See Table 7-4 for default conditions after a RESET instruction has occurred.

7.6 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits of the PCON register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Word 2. See Section 3.4.2 "Overflow/Underflow Reset" for more information.

7.7 Programming Mode Exit

Upon exit of Programming mode, the device will behave as if a POR had just occurred.

7.8 Power-Up Timer

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow VDD to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the $\overrightarrow{\text{PWRTE}}$ bit of Configuration Word 1.

7.9 Start-up Sequence

Upon the release of a POR or BOR, the following must occur before the device will begin executing:

- 1. Power-up Timer runs to completion (if enabled).
- 2. Oscillator start-up timer runs to completion (if required for oscillator source).
- 3. MCLR must be released (if enabled).

The total time-out will vary based on oscillator configuration and Power-up Timer configuration. See Section 5.0 "Oscillator Module (With Fail-Safe Clock Monitor)" for more information.

The Power-up Timer and oscillator start-up timer run independently of MCLR Reset. If MCLR is kept low long enough, the Power-up Timer and oscillator start-up timer will expire. Upon bringing MCLR high, the device will begin execution immediately (see Figure 7-4). This is useful for testing purposes or to synchronize more than one device operating in parallel.

PIC16F/LF1825/1829

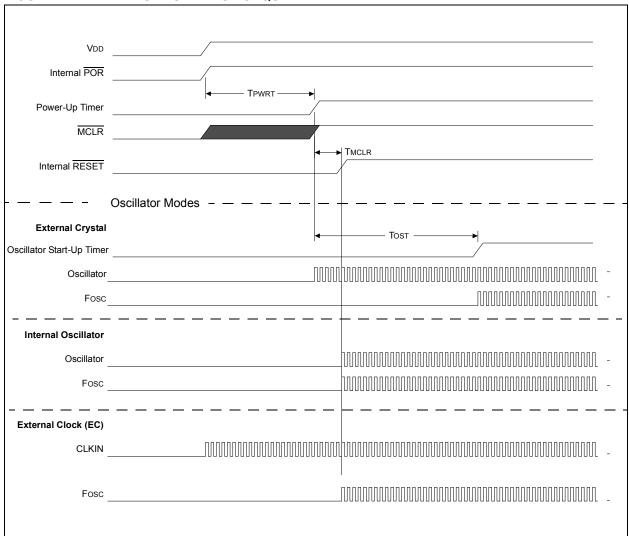


FIGURE 7-4: RESET START-UP SEQUENCE

7.10 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON register are updated to indicate the cause of the Reset. Table 7-3 and Table 7-4 show the Reset conditions of these registers.

STKOVF	STKUNF	RMCLR	RI	POR	BOR	то	PD	Condition
0	0	1	1	0	х	1	1	Power-on Reset
0	0	1	1	0	х	0	х	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	0	1	1	0	х	х	0	Illegal, \overline{PD} is set on \overline{POR}
0	0	1	1	u	0	1	1	Brown-out Reset
u	u	u	u	u	u	0	u	WDT Reset
u	u	u	u	u	u	0	0	WDT Wake-up from Sleep
u	u	u	u	u	u	1	0	Interrupt Wake-up from Sleep
u	u	0	u	u	u	u	u	MCLR Reset during normal operation
u	u	0	u	u	u	1	0	MCLR Reset during Sleep
u	u	u	0	u	u	u	u	RESET Instruction Executed
1	u	u	u	u	u	u	u	Stack Overflow Reset (STVREN = 1)
u	1	u	u	u	u	u	u	Stack Underflow Reset (STVREN = 1)

TABLE 7-3: RESET STATUS BITS AND THEIR SIGNIFICANCE

TABLE 7-4: RESET CONDITION FOR SPECIAL REGISTERS⁽²⁾

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	1 1000	00 110x
MCLR Reset during normal operation	0000h	u uuuu	uu Ouuu
MCLR Reset during Sleep	0000h	1 Ouuu	uu Ouuu
WDT Reset	0000h	0 uuuu	uu uuuu
WDT Wake-up from Sleep	PC + 1	0 Ouuu	uu uuuu
Brown-out Reset	0000h	1 luuu	00 11u0
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	1 Ouuu	uu uuuu
RESET Instruction Executed	0000h	u uuuu	uu u0uu
Stack Overflow Reset (STVREN = 1)	0000h	u uuuu	1u uuuu
Stack Underflow Reset (STVREN = 1)	0000h	u uuuu	ul uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

2: If a Status bit is not implemented, that bit will be read as '0'.

7.11 Power Control (PCON) Register

The Power Control (PCON) register contains flag bits to differentiate between a:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Reset Instruction Reset (RI)
- Stack Overflow Reset (STKOVF)
- Stack Underflow Reset (STKUNF)
- MCLR Reset (RMCLR)

The PCON register bits are shown in Register 7-2.

REGISTER 7-2: PCON: POWER CONTROL REGISTER

R/W/HS-0/q	R/W/HS-0/q	U-0	U-0	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-q/u	R/W/HC-q/u
STKOVF	STKUNF	—	—	RMCLR	RI	POR	BOR
bit 7							bit 0

Legend:				
HC = Bit is cle	ared by hardw	are	HS = Bit is set by hardware	
R = Readable	bit	W = Writable bit	U = Unimplemented bit, read as '0'	
u = Bit is unchanged x = Bit is unkno		x = Bit is unknown	-m/n = Value at POR and BOR/Value at all other Resets	
'1' = Bit is set '0' = Bit is clear		'0' = Bit is cleared	q = Value depends on condition	
bit 7	1 = A Stack	ack Overflow Flag bit Overflow occurred Overflow has not occurred o	or set to '0' by firmware	
bit 6	1 = A Stack	ack Underflow Flag bit Underflow occurred Underflow has not occurred	l or set to '0' by firmware	
bit 5-4	Unimpleme	nted: Read as '0'		
bit 3	RMCLR: MC	LR Reset Flag bit		
		Reset has not occurred or s Reset has occurred (set to	set to '1' by firmware '0' in hardware when a MCLR Reset occurs)	
bit 2	RI: RESET IN	struction Flag bit		
			ecuted or set to '1' by firmware ed (set to '0' in hardware upon executing a RESET instruction)	
bit 1	POR: Power	on Reset Status bit		
 1 = No Power-on Reset occurred 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs) 				
bit 0 BOR: Brown-out Reset Status bit				
 1 = No Brown-out Reset occurred 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out I occurs) 				

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	_	_		_		_	BORRDY	81
PCON	STKOVF	STKUNF	_	_	RMCLR	RI	POR	BOR	85
STATUS	_	_	_	TO	PD	Z	DC	С	26
WDTCON	_		WDTPS4	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	107

TABLE 7-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Legend: — = unimplemented bit, reads as '0'. Shaded cells are not used by Resets.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

8.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

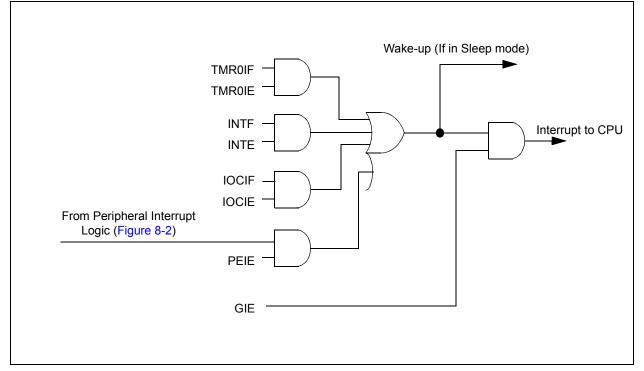
This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- · Automatic Context Saving

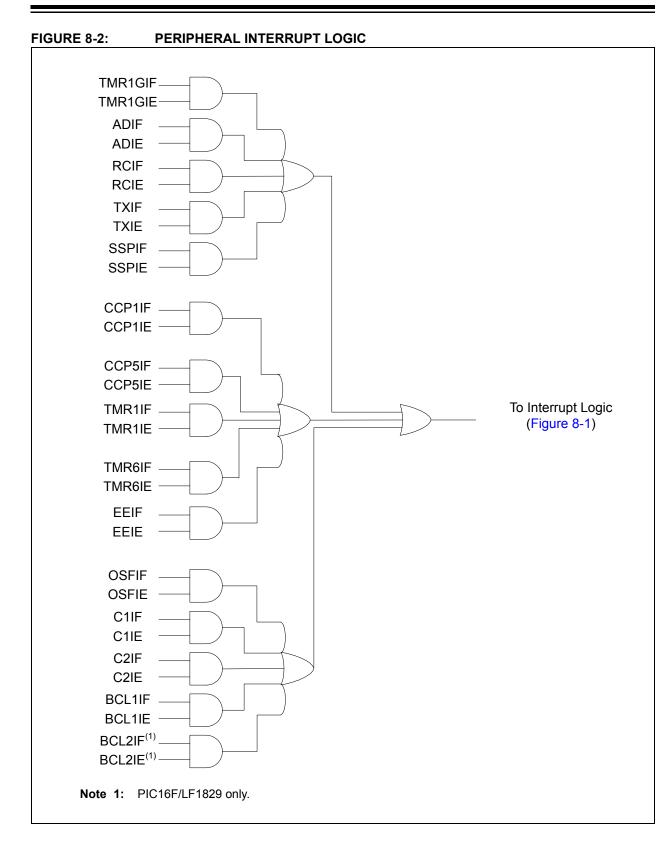
Many peripherals produce Interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 8-1 and Figure 8-2.





PIC16F/LF1825/1829



8.1 Operation

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt Enable bit(s) for the specific interrupt event(s)
- PEIE bit of the INTCON register (if the Interrupt Enable bit of the interrupt event is contained in the PIEx register)

The INTCON, PIR1, PIR2, PIR3 and PIR4 registers record individual interrupts via interrupt flag bits. Interrupt flag bits will be set, regardless of the status of the GIE, PEIE and individual interrupt enable bits.

The following events happen when an interrupt event occurs while the GIE bit is set:

- Current prefetched instruction is flushed
- · GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- Critical registers are automatically saved to the shadow registers (See Section 8.5 "Automatic Context Saving")
- PC is loaded with the interrupt vector 0004h

The firmware within the Interrupt Service Routine (ISR) should determine the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

The RETFIE instruction exits the ISR by popping the previous address from the stack, restoring the saved context from the shadow registers and setting the GIE bit.

For additional information on a specific interrupt's operation, refer to its peripheral chapter.

Note 1:	Individual	inte	rrupt	flag	bits	are	set,
	regardless	of	the	state	of	any	other
	enable bits						

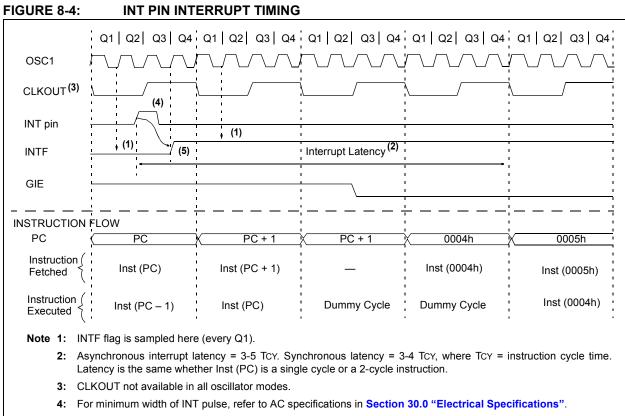
2: All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again.

8.2 Interrupt Latency

Interrupt latency is defined as the time from when the interrupt event occurs to the time code execution at the interrupt vector begins. The latency for synchronous interrupts is 3 or 4 instruction cycles. For asynchronous interrupts, the latency is 3 to 5 instruction cycles, depending on when the interrupt occurs. See Figure 8-3 and Figure 8.3 for more details.

PIC16F/LF1825/1829

FIGURE	8-3: I	NTERRUPT						
OSC1								
	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
CLKOUT			Interru during	pt Sampled Q1				
Interrupt								
GIE								
PC	PC-1	PC	PC	+1	0004h	0005h		
Execute	1 Cycle Inst	ruction at PC	Inst(PC)	NOP	NOP	Inst(0004h)		
Interrupt								
GIE								
PC	PC-1	PC	PC+1/FSR ADDR	New PC/ PC+1	0004h	0005h		
Execute-	2 Cycle Instr	ruction at PC	Inst(PC)	NOP	NOP	Inst(0004h)		
Interrupt								
GIE								
PC	PC-1	PC	FSR ADDR	PC+1	PC+2	0004h	0005h	
Execute	3 Cycle Inst	ruction at PC	INST(PC)	NOP	NOP	NOP	Inst(0004h)	Inst(0005h)
Interrupt								
GIE								
PC	PC-1	PC	FSR ADDR	PC+1	PC	+2	0004h	0005h
Execute	3 Cycle Inst	ruction at PC	INST(PC)	NOP	NOP	NOP	NOP	Inst(0004h)



5: INTF is enabled to be set any time during the Q4-Q1 cycles.

8.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to the Section 9.0 "Power-Down Mode (Sleep)" for more details.

8.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

8.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the Shadow registers:

- W register
- STATUS register (except for TO and PD)
- · BSR register
- · FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding Shadow register should be modified and the value will be restored when exiting the ISR. The Shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

8.5.1 INTCON REGISTER

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, interrupt-on-change and external INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 8-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R-0/0						
GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF ⁽¹⁾
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	GIE: Global Interrupt Enable bit
	1 = Enables all active interrupts0 = Disables all interrupts
bit 6	PEIE: Peripheral Interrupt Enable bit 1 = Enables all active peripheral interrupts 0 = Disables all peripheral interrupts
bit 5	TMR0IE: Timer0 Overflow Interrupt Enable bit 1 = Enables the Timer0 interrupt 0 = Disables the Timer0 interrupt
bit 4	INTE: INT External Interrupt Enable bit 1 = Enables the INT external interrupt 0 = Disables the INT external interrupt
bit 3	IOCIE: Interrupt-on-Change Enable bit 1 = Enables the interrupt-on-change 0 = Disables the interrupt-on-change
bit 2	TMR0IF: Timer0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed 0 = TMR0 register did not overflow
bit 1	INTF: INT External Interrupt Flag bit 1 = The INT external interrupt occurred 0 = The INT external interrupt did not occur
bit 0	IOCIF: Interrupt-on-Change Interrupt Flag bit ⁽¹⁾ 1 = When at least one of the interrupt-on-change pins changed state 0 = None of the interrupt-on-change pins have changed state
Note 1:	The IOCIE Flag bit is read-only and cleared when all the Interrupt-on-Change flags in the IOCxE register

Note 1: The IOCIF Flag bit is read-only and cleared when all the Interrupt-on-Change flags in the IOCxF register have been cleared by software.

PIC16F/LF1825/1829

8.5.2 PIE1 REGISTER

The PIE1 register contains the interrupt enable bits, as shown in Register 8-2.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 8-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

| R/W-0/0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE |
| bit 7 | | | | | | | bit 0 |

Legend:								
R = Readable	bit	W = Writable bit	U = Unimplemented bit, read as '0'					
u = Bit is unchanged		x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets					
'1' = Bit is set		'0' = Bit is cleared						
bit 7	TMR1GIE: Ti	mer1 Gate Interrupt Enable b	bit					
		he Timer1 Gate Acquisition i	I					
		the Timer1 Gate Acquisition						
bit 6		onverter (ADC) Interrupt Ena	ble bit					
		he ADC interrupt						
1.11 E		the ADC interrupt						
bit 5		T Receive Interrupt Enable b	It					
		ne USART receive interrupt ne USART receive interrupt						
bit 4		Transmit Interrupt Enable bit						
	1 = Enables t	he USART transmit interrupt						
	0 = Disables	the USART transmit interrup	t					
bit 3	SSP1IE: Syne	chronous Serial Port (MSSP)	Interrupt Enable bit					
		he MSSP interrupt						
		the MSSP interrupt						
bit 2		P1 Interrupt Enable bit						
		he CCP1 interrupt						
L:1 4		the CCP1 interrupt						
bit 1		R2 to PR2 Match Interrupt Er						
		he Timer2 to PR2 match inte the Timer2 to PR2 match inte	•					
bit 0		er1 Overflow Interrupt Enable						
Sit U		he Timer1 overflow interrupt						
		the Timer1 overflow interrupt						
		•						

8.5.3 PIE2 REGISTER

The PIE2 register contains the interrupt enable bits, as shown in Register 8-3.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 8-3: PIEZ: PERIPHERAL INTERRUPT ENABLE REGISTER 2	REGISTER 8-3:	PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2
--	---------------	--

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0
OSFIE	C2IE ⁽¹⁾	C1IE	EEIE	BCL1IE	—	—	CCP2IE
bit 7							bit 0

Legend:					
R = Readable	R = Readable bit W = Writable		U = Unimplemented bit, read as '0'		
u = Bit is unch	nanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets		
'1' = Bit is set		'0' = Bit is cleared			
bit 7	OSFIE: Osci	illator Fail Interrupt Enable I	bit		
	1 = Enables	the Oscillator Fail interrupt	t		
		s the Oscillator Fail interrup			
bit 6	C2IE: Comp	arator C2 Interrupt Enable I	bit ⁽¹⁾		
		the Comparator C2 interru	•		
	0 = Disables the Comparator C2 interrupt				
bit 5	- Frank - Fran				
 1 = Enables the Comparator C1 interrupt 0 = Disables the Comparator C1 interrupt 					
bit 4	EEIE: EEPROM Write Completion Interrupt Enable bit				
	1 = Enables the EEPROM Write Completion Interrupt				
	0 = Disables the EEPROM Write Completion interrupt				
bit 3	BCL1IE: MSSP Bus Collision Interrupt Enable bit				
	1 = Enables	the MSSP Bus Collision In	iterrupt		
	0 = Disables the MSSP Bus Collision Interrupt				
bit 2-1	Unimplemented: Read as '0'				
bit 0	CCP2IE: CCP2 Interrupt Enable bit				
		the CCP2 Interrupt			
	0 = Disables	s the CCP2 Interrupt			
Note 1: PIC	C16F/LF1829 c	only.			
		•			

PIC16F/LF1825/1829

8.5.4 PIE3 REGISTER

The PIE3 register contains the interrupt enable bits, as shown in Register 8-4.

Note 1: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 8-4:	PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	U-0
—	—	CCP4IE	CCP3IE	TMR6IE	—	TMR4IE	—
bit 7							bit 0

Legend:					
R = Readable bit		W = Writable bit	U = Unimplemented bit, read as '0'		
u = Bit is u	nchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets		
'1' = Bit is set		'0' = Bit is cleared			
bit 7-6	Unimplem	nented: Read as '0'			
bit 5	CCP4IE: (CCP4 Interrupt Enable bit			
1 = Enables the CCP4 interrupt0 = Disables the CCP4 interrupt					
bit 4	CCP3IE: CCP3 Interrupt Enable bit				
		es the CCP3 interrupt les the CCP3 interrupt			
bit 3	TMR6IE: TMR6 to PR6 Match Interrupt Enable bit				
	 1 = Enables the TMR6 to PR6 Match interrupt 0 = Disables the TMR6 to PR6 Match interrupt 				
bit 2	Unimplem	Unimplemented: Read as '0'			
bit 1	TMR4IE:	TMR4 to PR4 Match Interrup	ot Enable bit		
		es the TMR4 to PR4 Match les the TMR4 to PR4 Match			

bit 0 Unimplemented: Read as '0'

8.5.5 PIE4 REGISTER⁽¹⁾

The PIE4 register contains the interrupt enable bits, as shown in Register 8-5.

- Note 1: The PIE4 register is available only on the PIC16F/LF1829 device.
 - 2: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 8-5: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	—	_	—	—	BCL2IE	SSP2IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2	Unimplemented: Read as '0'
bit 1	BCL2IE: MSSP2 Bus Collision Interrupt Enable bit
	 1 = Enables the MSSP2 Bus Collision Interrupt 0 = Disables the MSSP2 Bus Collision Interrupt
bit 0	 SSP2IE: Master Synchronous Serial Port 2 (MSSP2) Interrupt Enable bit 1 = Enables the MSSP2 interrupt 0 = Disables the MSSP2 interrupt

Note 1: This register is only available on PIC16F/LF1829.

PIC16F/LF1825/1829

8.5.6 PIR1 REGISTER

The PIR1 register contains the interrupt flag bits, as shown in Register 8-6.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 8-6: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	TMR1GIF: Timer1 Gate Interrupt Flag bit
	1 = Interrupt is pending
	0 = Interrupt is not pending
bit 6	ADIF: A/D Converter Interrupt Flag bit
	1 = Interrupt is pending
	0 = Interrupt is not pending
bit 5	RCIF: USART Receive Interrupt Flag bit
	1 = Interrupt is pending
	0 = Interrupt is not pending
bit 4	TXIF: USART Transmit Interrupt Flag bit
	1 = Interrupt is pending
	0 = Interrupt is not pending
bit 3	SSP1IF: Synchronous Serial Port (MSSP) Interrupt Flag bit
	1 = Interrupt is pending
	0 = Interrupt is not pending
bit 2	CCP1IF: CCP1 Interrupt Flag bit
	1 = Interrupt is pending
	0 = Interrupt is not pending
bit 1	TMR2IF: Timer2 to PR2 Interrupt Flag bit
	1 = Interrupt is pending
	0 = Interrupt is not pending
bit 0	TMR1IF: Timer1 Overflow Interrupt Flag bit
	1 = Interrupt is pending
	0 = Interrupt is not pending

8.5.7 PIR2 REGISTER

The PIR2 register contains the interrupt flag bits, as shown in Register 8-7.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 8-7: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0
OSFIF	C2IF ⁽¹⁾	C1IF	EEIF	BCL1IF	—	—	CCP2IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

b	oit 7	OSFIF: Oscillator Fail Interrupt Flag bit
		1 = Interrupt is pending
		0 = Interrupt is not pending
b	oit 6	C2IF: Comparator C2 Interrupt Flag bit ⁽¹⁾
		1 = Interrupt is pending
		0 = Interrupt is not pending
b	oit 5	C1IF: Comparator C1 Interrupt Flag bit
		1 = Interrupt is pending
		0 = Interrupt is not pending
b	oit 4	EEIF: EEPROM Write Completion Interrupt Flag bit
		1 = Interrupt is pending
		0 = Interrupt is not pending
b	it 3	BCL1IF: MSSP Bus Collision Interrupt Flag bit
		1 = Interrupt is pending
		0 = Interrupt is not pending
b	it 2-1	CCP2IF: CCP2 Interrupt Flag bit
		1 = Interrupt is pending
		0 = Interrupt is not pending
b	oit O	Unimplemented: Read as '0'
Ν	lote 1: PIC	16F/LF1829 only.
	-	, , , , , , , , , , , , , , , , , , ,

8.5.8 PIR3 REGISTER

The PIR3 register contains the interrupt flag bits, as shown in Register 8-8.

Note 1: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 8-8: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	U-0
—	—	CCP4IF	CCP3IF	TMR6IF	—	TMR4IF	—
bit 7							bit 0

Legend:						
R = Readable bit		W = Writable bit	U = Unimplemented bit, read as '0'			
u = Bit is unch	anged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets			
'1' = Bit is set		'0' = Bit is cleared				
bit 7-6	Unimplemen	nted: Read as '0'				
bit 5	CCP4IF: CCI	P4 Interrupt Flag bit				
	1 = Interrupt	is pending				
	0 = Interrupt	is not pending				
bit 4	CCP3IF: CCI	P3 Interrupt Flag bit				
	1 = Interrupt	is pending				
	0 = Interrupt is not pending					
bit 3	TMR6IF: TMR6 to PR6 Match Interrupt Flag bit					
1 = Interrupt is pending						
0 = Interrupt is not pending						
bit 2	Unimplemented: Read as '0'					

- bit 1 TMR4IF: TMR4 to PR4 Match Interrupt Flag bit
 - 1 = Interrupt is pending
 0 = Interrupt is not pending
- bit 0 Unimplemented: Read as '0'

8.5.9 PIR4 REGISTER⁽¹⁾

The PIR4 register contains the interrupt flag bits, as shown in Register 8-9.

- **Note 1:** The PIR4 register is available only on the PIC16F/LF1829 device.
 - 2: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 8-9: PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	—	—	—	BCL2IF	SSP2IF
bit 7							bit 0

Legend:								
R = Reada	ble bit	W = Writable bit	U = Unimplemented bit, read as '0'					
u = Bit is unchanged		x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Rese					
'1' = Bit is set		'0' = Bit is cleared	HS = Bit is set by hardware					
bit 7-6	Unimpler	nented: Read as '0'						
bit 1	BCI 2IF: MSSP2 Bus Collision Interrupt Flag bit							

bit 1	BCL2IF: MSSP2 Bus Collision Interrupt Flag bit
	 1 = A Bus Collision was detected (must be cleared in software) 0 = No Bus collision was detected
bit 0	SSP2IF: Master Synchronous Serial Port 2 (MSSP2) Interrupt Flag bit
	 1 = The Transmission/Reception/Bus Condition is complete (must be cleared in software) 0 = Waiting to Transmit/Receive/Bus Condition in progress

Note 1: This register is only available on PIC16F/LF1829.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA	PS2	PS1	PS0	189
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	-	_	CCP2IE	95
PIE3	—	-	CCP4IE	CCP3IE	TMR6IE	-	TMR4IE	_	96
PIE4 ⁽¹⁾	—		_	_	-		BCL2IE	SSP2IE	97
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF		_	CCP2IF	99
PIR3	_	_	CCP4IF	CCP3IF	TMR6IF	_	TMR4IF	_	100
PIR4 ⁽¹⁾	_	_	_	_	_	_	BCL2IF	SSP2IF	101

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Legend: — = unimplemented locations read as '0'. Shaded cells are not used by Interrupts.

Note 1: PIC16F/LF1829 only.

9.0 POWER-DOWN MODE (SLEEP)

The Power-Down mode is entered by executing a SLEEP instruction.

Upon entering Sleep mode, the following conditions exist:

- 1. WDT will be cleared but keeps running, if enabled for operation during Sleep.
- 2. PD bit of the STATUS register is cleared.
- 3. $\overline{\text{TO}}$ bit of the STATUS register is set.
- 4. CPU clock is disabled.
- 5. 31 kHz LFINTOSC is unaffected and peripherals that operate from it may continue operation in Sleep.
- 6. Timer1 oscillator is unaffected and peripherals that operate from it may continue operation in Sleep.
- 7. ADC is unaffected, if the dedicated FRC clock is selected.
- 8. Capacitive Sensing oscillator is unaffected.
- I/O ports maintain the status they had before SLEEP was executed (driving high, low or highimpedance).
- 10. Resets other than WDT are not affected by Sleep mode.

Refer to individual chapters for more details on peripheral operation during Sleep.

To minimize current consumption, the following conditions should be considered:

- I/O pins should not be floating
- External circuitry sinking current from I/O pins
- Internal circuitry sourcing current from I/O pins
- · Current draw from pins with internal weak pull-ups
- Modules using 31 kHz LFINTOSC
- Modules using Timer1 oscillator

I/O pins that are high-impedance inputs should be pulled to VDD or VSS externally to avoid switching currents caused by floating inputs.

Examples of internal circuitry that might be sourcing current include modules such as the DAC and FVR modules. See Section 17.0 "Digital-to-Analog Converter (DAC) Module" and Section 14.0 "Fixed Voltage Reference (FVR)" for more information on these modules.

9.1 Wake-up from Sleep

The device can wake-up from Sleep through one of the following events:

- 1. External Reset input on MCLR pin, if enabled
- 2. BOR Reset, if enabled
- 3. POR Reset
- 4. Watchdog Timer, if enabled
- 5. Any external interrupt
- 6. Interrupts by peripherals capable of running during Sleep (see individual peripheral for more information)

The first three events will cause a device Reset. The last three events are considered a continuation of program execution. To determine whether a device Reset or wake-up event occurred, refer to Section 7.10 "Determining the Cause of a Reset".

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be enabled. Wake-up will occur regardless of the state of the GIE bit. If the GIE bit is disabled, the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is enabled, the device executes the instruction after the SLEEP instruction, the device will call the Interrupt Service Routine. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

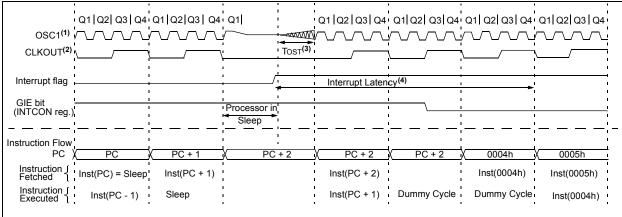
9.1.1 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction
 - SLEEP instruction will execute as a NOP.
 - WDT and WDT prescaler will not be cleared
 - TO bit of the STATUS register will not be set
 - PD bit of the STATUS register will not be cleared.
- If the interrupt occurs **during or after** the execution of a **SLEEP** instruction
 - SLEEP instruction will be completely executed
 - Device will immediately wake-up from Sleep
 - WDT and WDT prescaler will be cleared
 - TO bit of the STATUS register will be set
 - PD bit of the STATUS register will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

FIGURE 9-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP Oscillator mode assumed.

2: CLKOUT is not available in XT, HS, or LP Oscillator modes, but shown here for timing reference.

3: TOST = 1024 TOSC (drawing not to scale). This delay applies only to XT, HS or LP Oscillator modes.

4: GIE = 1 assumed. In this case after wake-up, the processor calls the ISR at 0004h. If GIE = 0, execution will continue in-line.

TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
IOCAF	_	_	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	144
IOCAN	_	_	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	144
IOCAP	_	_	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	144
IOCBF ⁽¹⁾	IOCBF7	IOCBF6	IOCBF5	IOCBF4	_	_	—	_	146
IOCBN ⁽¹⁾	IOCBN7	IOCBN6	IOCBN5	IOCBN4	—	—	—	—	145
IOCBP ⁽¹⁾	IOCBP7	IOCBP6	IOCBP5	IOCBP4	—	—	—	—	145
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	95
PIE4 ⁽¹⁾	—	_	_	—	—	_	BCL2IE	SSP2IE	97
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	99
PIR4 ⁽¹⁾	—	—	—	—	—	—	BCL2IF	SSP2IF	101
STATUS	_	_	_	TO	PD	Z	DC	С	26
WDTCON	—	_	WDTPS4	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	107

Legend: — = unimplemented, read as '0'. Shaded cells are not used in Power-down mode. Note 1: PIC16F/LF1829 only.

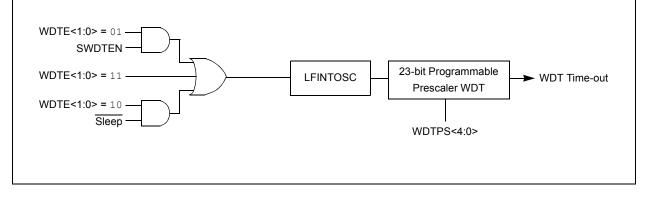
10.0 WATCHDOG TIMER

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- · Independent clock source
- Multiple operating modes
 - WDT is always on
 - WDT is off when in Sleep
 - WDT is controlled by software
 - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (typical)
- Multiple Reset conditions
- Operation during Sleep

FIGURE 10-1: WATCHDOG TIMER BLOCK DIAGRAM



10.1 Independent Clock Source

The WDT derives its time base from the 31 kHz LFINTOSC internal oscillator.

10.2 WDT Operating Modes

The Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Word 1. See Table 10-1.

10.2.1 WDT IS ALWAYS ON

When the WDTE bits of Configuration Word 1 are set to '11', the WDT is always on.

WDT protection is active during Sleep.

10.2.2 WDT IS OFF IN SLEEP

When the WDTE bits of Configuration Word 1 are set to '10', the WDT is on, except in Sleep.

WDT protection is not active during Sleep.

10.2.3 WDT CONTROLLED BY SOFTWARE

When the WDTE bits of Configuration Word 1 are set to '01', the WDT is controlled by the SWDTEN bit of the WDTCON register.

WDT protection is unchanged by Sleep. See Table 10-1 for more details.

WDTE Config bits	SWDTEN	Device Mode	WDT Mode
WDT_ON (11)	Х	Х	Active
WDT_NSLEEP (10)	Х	Awake	Active
WDT_NSLEEP (10)	Х	Sleep	Disabled
WDT_SWDTEN (01)	1	Х	Active
WDT_SWDTEN (01)	0	Х	Disabled
WDT_OFF (00)	Х	Х	Disabled

TABLE 10-1: WDT OPERATING MODES

10.3 Time-Out Period

The WDTPS bits of the WDTCON register set the time-out period from 1 ms to 256 seconds. After a Reset, the default time-out period is 2 seconds.

10.4 Clearing the WDT

The WDT is cleared when any of the following conditions occur:

- Any Reset
- CLRWDT instruction is executed
- · Device enters Sleep
- · Device wakes up from Sleep
- Oscillator fail event
- WDT is disabled
- Oscillator Start-up TImer (OST) is running

See Table 10-2 for more information.

10.5 Operation During Sleep

When the device enters Sleep, the WDT is cleared. If the WDT is enabled during Sleep, the WDT resumes counting.

When the device exits Sleep, the WDT is cleared again. The WDT remains clear until the OST, if enabled, completes. See Section 5.0 "Oscillator Module (With Fail-Safe Clock Monitor)" for more information on the OST.

When a WDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the <u>device</u> wakes up and resumes operation. The <u>TO</u> and <u>PD</u> bits in the STATUS register are changed to indicate the event. See <u>Section 3.0</u> "Memory Organization" for more information.

TABLE 10-2: WDT CLEARING CONDITIONS

Conditions	WDT	
WDTE<1:0> = 00		
WDTE<1:0> = 01 and SWDTEN = 0		
WDTE<1:0> = 10 and enter Sleep	Cleared	
CLRWDT Command	Cleared	
Oscillator Fail Detected		
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK		
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST	
Change INTOSC divider (IRCF bits)	Unaffected	

U-0	U-0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0	
_				WDTPS<4:0			SWDTEN	
oit 7							bit	
Legend:								
R = Readable bit W = Writab			bit	U = Unimpler	mented bit, read	d as '0'		
u = Bit is unchanged		x = Bit is unknown		-m/n = Value at POR and BOR/Value at all of			other Resets	
'1' = Bit is set		'0' = Bit is cle	'0' = Bit is cleared					
bit 7-6	Unimplem	ented: Read as '	0'					
bit 5-1	WDTPS<4:0>: Watchdog Timer Period Select bits							
	Bit Value = Prescale Rate							
	00000 = 1:32 (Interval 1 ms typ)							
	00001 =	1:64 (Interval 2 m	s typ)					
	00010 = 1:128 (Interval 4 ms typ)							
	00011 = 1:256 (Interval 8 ms typ) 00100 = 1:512 (Interval 16 ms typ)							
	00100 = 1.512 (Interval 18 his typ) 00101 = 1:1024 (Interval 32 ms typ)							
	00110 = 1:2048 (Interval 64 ms typ)							
		00111 = 1:4096 (Interval 128 ms typ)						
		01000 = 1:8192 (Interval 256 ms typ)						
	01001 = 1:16384 (Interval 512 ms typ) 01010 = 1:32768 (Interval 1s typ)							
	01010 = 1.65536 (Interval 2s typ) (Reset value)							
	01100 = '	01100 = 1:131072 (2^{17}) (Interval 4s typ) 01101 = 1:262144 (2^{18}) (Interval 8s typ)						
	01101 = $1:262144 (2^{18})$ (Interval 8s typ)							
	$01110 = 1:524288 (2^{19}) (Interval 16s typ)$							
	01111 = 1:1048576 (2 ²⁰) (Interval 32s typ) 10000 = 1:2097152 (2 ²¹) (Interval 64s typ)							
		1:4194304 (2 ²²) (
	10010 =	1:8388608 (2 ²³) (Interval 256s	typ)				
	10011 = Reserved. Results in minimum interval (1:32)							
	•							
	•							
	11111 = Reserved. Results in minimum interval (1:32)							
bit 0	SWDTEN: Software Enable/Disable for Watchdog Timer bit							
	<u>If WDTE<1:0> = 00</u> :							
	This bit is ignored.							
	If WDTE<1							
		s turned on s turned off						
	0 = WDTT <u>If WDTE<1</u>							
	This bit is i	$\cdot \mathbf{v}^{\prime} = 1 \mathbf{\Lambda}$						

REGISTER 10-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

NOTES:

11.0 DATA EEPROM AND FLASH PROGRAM MEMORY CONTROL

The data EEPROM and Flash program memory are readable and writable during normal operation (full VDD range). These memories are not directly mapped in the register file space. Instead, they are indirectly addressed through the Special Function Registers (SFRs). There are six SFRs used to access these memories:

- EECON1
- EECON2
- EEDATL
- EEDATH
- EEADRL
- EEADRH

When interfacing the data memory block, EEDATL holds the 8-bit data for read/write, and EEADRL holds the address of the EEDATL location being accessed. These devices have 256 bytes of data EEPROM with an address range from 0h to 0FFh.

When accessing the program memory block, the EED-ATH:EEDATL register pair forms a 2-byte word that holds the 14-bit data for read/write, and the EEADRL and EEADRH registers form a 2-byte word that holds the 15-bit address of the program memory location being read.

The EEPROM data memory allows byte read and write. An EEPROM byte write automatically erases the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

Depending on the setting of the Flash Program Memory Self Write Enable bits WRT<1:0> of the Configuration Word 2, the device may or may not be able to write certain blocks of the program memory. However, reads from the program memory are always allowed.

When the device is code-protected, the device programmer can no longer access data or program memory. When code-protected, the CPU may continue to read and write the data EEPROM memory and Flash program memory.

11.1 EEADRL and EEADRH Registers

The EEADRH:EEADRL register pair can address up to a maximum of 256 bytes of data EEPROM or up to a maximum of 32K words of program memory.

When selecting a program address value, the MSB of the address is written to the EEADRH register and the LSB is written to the EEADRL register. When selecting a EEPROM address value, only the LSB of the address is written to the EEADRL register.

11.1.1 EECON1 AND EECON2 REGISTERS

EECON1 is the control register for EE memory accesses.

Control bit EEPGD determines if the access will be a program or data memory access. When clear, any subsequent operations will operate on the EEPROM memory. When set, any subsequent operations will operate on the program memory. On Reset, EEPROM is selected by default.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to occur. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and execute the appropriate error handling routine.

Interrupt flag bit EEIF of the PIR2 register is set when write is complete. It must be cleared in the software.

Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence. To enable writes, a specific pattern must be written to EECON2.

11.2 Using the Data EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM without exceeding the total number of write cycles to a single byte. Refer to Section 30.0 "Electrical Specifications". If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

11.2.1 READING THE DATA EEPROM MEMORY

To read a data memory location, the user must write the address to the EEADRL register, clear the EEPGD and CFGS control bits of the EECON1 register, and then set control bit RD. The data is available at the very next cycle, in the EEDATL register; therefore, it can be read in the next instruction. EEDATL will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 11-1: DATA EEPROM READ

BANKSEL	EEADRL		;
MOVLW	DATA_EE	ADDR	;
MOVWF	EEADRL		;Data Memory
			;Address to read
BCF	EECON1,	CFGS	;Deselect Config space
BCF	EECON1,	EEPGI	;Point to DATA memory
BSF	EECON1,	RD	;EE Read
MOVF	EEDATL,	W	;W = EEDATL

Note: Data EEPROM can be read regardless of the setting of the CPD bit.

11.2.2 WRITING TO THE DATA EEPROM MEMORY

To write an EEPROM data location, the user must first write the address to the EEADRL register and the data to the EEDATL register. Then the user must follow a specific sequence to initiate the write for each byte.

The write will not initiate if the above sequence is not followed exactly (write 55h to EECON2, write AAh to EECON2, then set the WR bit) for each byte. Interrupts should be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

11.2.3 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built-in. On power-up, WREN is cleared. Also, the Power-up Timer (64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

- Brown-out
- Power Glitch
- · Software Malfunction

11.2.4 DATA EEPROM OPERATION DURING CODE-PROTECT

Data memory can be code-protected by programming the \overline{CPD} bit in the Configuration Word 1 (Register 5-1) to '0'.

When the data memory is code-protected, only the CPU is able to read and write data to the data EEPROM. It is recommended to code-protect the program memory when code-protecting data memory. This prevents anyone from replacing your program with a program that will access the contents of the data EEPROM.

	BANKSEL	EEADRL	;
	MOVLW	DATA_EE_AD	DR ;
	MOVWF	EEADRL	;Data Memory Address to write
	MOVLW	DATA_EE_DA	TA ;
	MOVWF	EEDATL	;Data Memory Value to write
	BCF	EECON1, CF	GS ;Deselect Configuration space
	BCF	EECON1, EE	PGD ;Point to DATA memory
	BSF	EECON1, WR	EN ;Enable writes
	BCF	INTCON, GI	E ;Disable INTs.
	MOVLW	55h	;
Required Sequence	MOVWF	EECON2	;Write 55h
uire Len	MOVLW	0AAh	;
Sec	MOVWF	EECON2	;Write AAh
ш о	BSF	EECON1, WR	;Set WR bit to begin write
	BSF	INTCON, GI	E ;Enable Interrupts
	BCF	EECON1, WR	EN ;Disable writes
	BTFSC	EECON1, WR	;Wait for write to complete
	GOTO	\$-2	;Done
1			



	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
Flash ADDR	PC	PC + 1	EEADRH,EEADRL	PC + 3	PC + 4	PC + 5
Flash Data			R (PC + 1) EEDA		R (PC + 3) INST	R (PC + 4)
	INSTR(PC - 1) executed here	BSF EECON1,RD executed here	INSTR(PC + 1) executed here	Forced NOP executed here	INSTR(PC + 3) executed here	INSTR(PC + 4) executed here
RD bit		 	/			
EEDATH EEDATL Register				X		
EERHLT			/			

11.3 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum block size that can be erased by user software.

Flash program memory may only be written or erased if the destination address is in a segment of memory that is not write-protected, as defined in bits WRT<1:0> of Configuration Word 2.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the EEDATH:EEDATL register pair.

Note:	If the user wants to modify only a portion
	of a previously programmed row, then the
	contents of the entire row must be read
	and saved in RAM prior to the erase.

The number of data write latches is not equivalent to the number of row locations. During programming, user software will need to fill the set of write latches and initiate a programming operation multiple times in order to fully reprogram an erased row. For example, a device with a row size of 32 words and eight write latches will need to load the write latches with data and initiate a programming operation four times.

The size of a program memory row and the number of program memory write latches may vary by device. See Table 11-1 for details.

TABLE 11-1:FLASH MEMORY
ORGANIZATION BY DEVICE

Device	Erase Block (Row) Size/ Boundary	Number of Write Latches/ Boundary
PIC16F/LF1825/	32 words,	32 words,
1829	EEADRL<4:0>	EEADRL<4:0>
	= 00000	= 00000

11.3.1 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must:

- 1. Write the Least and Most Significant address bits to the EEADRH:EEADRL register pair.
- 2. Clear the CFGS bit of the EECON1 register.
- 3. Set the EEPGD control bit of the EECON1 register.
- 4. Then, set control bit RD of the EECON1 register.

Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "BSF EECON1, RD" instruction to be ignored. The data is available in the very next cycle, in the EEDATH:EEDATL register pair; therefore, it can be read as two bytes in the following instructions.

EEDATH:EEDATL register pair will hold this value until another read or until it is written to by the user.

- Note 1: The two instructions following a program memory read are required to be NOPS. This prevents the user from executing a two-cycle instruction on the next instruction after the RD bit is set.
 - 2: Flash program memory can be read regardless of the setting of the CP bit.

EXAMPLE 11-3: FLASH PROGRAM MEMORY READ

```
* This code block will read 1 word of program
* memory at the memory address:
   PROG ADDR HI : PROG ADDR LO
   data will be returned in the variables;
*
   PROG_DATA_HI, PROG_DATA_LO

      BANKSEL
      EEADRL
      ; Select Bank for EEPRO

      MOVLW
      PROG_ADDR_LO
      ;

      MOVWF
      EEADRL
      ; Store LSB of address

      MOVLW
      PROG_ADDR_HI
      ;

    BANKSEL EEADRL
                                    ; Select Bank for EEPROM registers
    MOVWL EEADRH
                                  ; Store MSB of address
             EECON1,CFGS ; Do not select Configuration Space
EECON1,EEPGD ; Select Program Memory
    BCF
             EECON1,CFGS
    BSF
               INTCON,GIE ; Disable interrupts
    BCF
    BSF
               EECON1,RD
                                    ; Initiate read
    NOP
                                    ; Executed (Figure 11-1)
    NOP
                                    ; Ignored (Figure 11-1)
    BSF
             INTCON, GIE
                                    ; Restore interrupts
    MOVF
             EEDATL,W
                                  ; Get LSB of word
    MOVWF
            PROG_DATA_LO ; Store in user location
                                 ; Get MSB of word
    MOVE
               EEDATH,W
             PROG DATA HI
    MOVWF
                                  ; Store in user location
```

11.3.2 ERASING FLASH PROGRAM MEMORY

While executing code, program memory can only be erased by rows. To erase a row:

- 1. Load the EEADRH:EEADRL register pair with the address of new row to be erased.
- 2. Clear the CFGS bit of the EECON1 register.
- 3. Set the EEPGD, FREE, and WREN bits of the EECON1 register.
- 4. Write 55h, then AAh, to EECON2 (Flash programming unlock sequence).
- 5. Set control bit WR of the EECON1 register to begin the erase operation.
- 6. Poll the FREE bit in the EECON1 register to determine when the row erase has completed.

See Example 11-4.

After the "BSF EECON1, WR" instruction, the processor requires two cycles to set up the erase operation. The user must place two NOP instructions after the WR bit is set. The processor will halt internal operations for the typical 2 ms erase time. This is not Sleep mode as the clocks and peripherals will continue to run. After the erase cycle, the processor will resume operation with the third instruction after the EECON1 write instruction.

11.3.3 WRITING TO FLASH PROGRAM MEMORY

Program memory is programmed using the following steps:

- 1. Load the starting address of the word(s) to be programmed.
- 2. Load the write latches with data.
- 3. Initiate a programming operation.
- 4. Repeat steps 1 through 3 until all data is written.

Before writing to program memory, the word(s) to be written must be erased or previously unwritten. Program memory can only be erased one row at a time. No automatic erase occurs upon the initiation of the write.

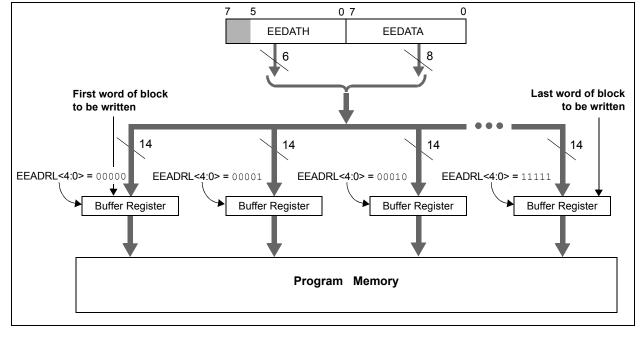
Program memory can be written one or more words at a time. The maximum number of words written at one time is equal to the number of write latches. See Figure 11-2 for more details. The write latches are aligned to the address boundary defined by EEADRL as shown in Table 11-1. Write operations do not cross these boundaries. At the completion of a program memory write operation, the write latches are reset to contain 0x3FFF. The following steps should be completed to load the write latches and program a block of program memory. These steps are divided into two parts. First, all write latches are loaded with data except for the last program memory location. Then, the last write latch is loaded and the programming sequence is initiated. A special unlock sequence is required to load a write latch with data or initiate a Flash programming operation. This unlock sequence should not be interrupted.

- 1. Set the EEPGD and WREN bits of the EECON1 register.
- 2. Clear the CFGS bit of the EECON1 register.
- Set the LWLO bit of the EECON1 register. When the LWLO bit of the EECON1 register is '1', the write sequence will only load the write latches and will not initiate the write to Flash program memory.
- 4. Load the EEADRH:EEADRL register pair with the address of the location to be written.
- 5. Load the EEDATH:EEDATL register pair with the program memory data to be written.
- Write 55h, then AAh, to EECON2, then set the WR bit of the EECON1 register (Flash programming unlock sequence). The write latch is now loaded.
- 7. Increment the EEADRH:EEADRL register pair to point to the next location.
- 8. Repeat steps 5 through 7 until all but the last write latch has been loaded.
- Clear the LWLO bit of the EECON1 register. When the LWLO bit of the EECON1 register is '0', the write sequence will initiate the write to Flash program memory.
- 10. Load the EEDATH:EEDATL register pair with the program memory data to be written.
- 11. Write 55h, then AAh, to EECON2, then set the WR bit of the EECON1 register (Flash programming unlock sequence). The entire latch block is now written to Flash program memory.

It is not necessary to load the entire write latch block with user program data. However, the entire write latch block will be written to program memory.

An example of the complete write sequence for eight words is shown in Example 11-5. The initial address is loaded into the EEADRH:EEADRL register pair; the eight words of data are loaded using indirect addressing. After the "BSF EECON1, WR" instruction, the processor requires two cycles to set up the write operation. The user must place two NOP instructions after the WR bit is set. The processor will halt internal operations for the typical 2 ms, only during the cycle in which the write takes place (i.e., the last word of the block write). This is not Sleep mode as the clocks and peripherals will continue to run. The processor does not stall when LWLO = 1, loading the write latches. After the write cycle, the processor will resume operation with the third instruction after the EECON1 write instruction.





PIC16F/LF1825/1829

EXAMPLE 11-4: ERASING ONE ROW OF PROGRAM MEMORY

; This row erase routine assumes the following:

; 1. A valid address within the erase block is loaded in ADDRH:ADDRL

; 2. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F

	BCF	INTCON, GIE	; Disable ints so required sequences will execute properly
	BANKSEL	EEADRL	
	MOVF	ADDRL,W	; Load lower 8 bits of erase address boundary
	MOVWF	EEADRL	
	MOVF	ADDRH,W	; Load upper 6 bits of erase address boundary
	MOVWF	EEADRH	
	BSF	EECON1, EEPGD	; Point to program memory
	BCF	EECON1,CFGS	; Not configuration space
	BSF	EECON1, FREE	; Specify an erase operation
	BSF	EECON1,WREN	; Enable writes
	MOVLW	55h	; Start of required sequence to initiate erase
	MOVWF	EECON2	; Write 55h
ed Se	MOVLW	0AAh	;
Required Sequence	MOVWF	EECON2	; Write AAh
equ	BSF	EECON1,WR	; Set WR bit to begin erase
шv	NOP		; Any instructions here are ignored as processor
			; halts to begin erase sequence
	NOP		; Processor will stop here and wait for erase complete.
L			
			; after erase processor continues with 3rd instruction
	DOE	DECOM1 MDEX	
	BCF		; Disable writes
	BSF	INTCON,GIE	; Enable interrupts

PIC16F/LF1825/1829

EXAMPLE 11-5: WRITING TO FLASH PROGRAM MEMORY

	LE 11-5:		
		ine assumes the f	
	_		led, starting at the address in DATA_ADDR
			ten is made up of two adjacent bytes in DATA_ADDR,
		ttle endian forma	
		-	e least significant bits = 000) is loaded in ADDRH:ADDRL in shared data memory 0x70 - 0x7F
; 4. Al	JUKH ANG AL	DRL are located i	III Shared data memory 0x70 - 0x7F
,	BCF	INTCON, GIE	; Disable ints so required sequences will execute properly
	BANKSEL	EEADRH	; Bank 3
	MOVF	ADDRH,W	; Load initial address
	MOVWF	EEADRH	:
	MOVE	ADDRL,W	;
	MOVWF	EEADRL	;
	MOVLW	LOW DATA ADDR	; Load initial data address
	MOVWF	FSROL	;
	MOVLW	HIGH DATA ADDR	; Load initial data address
	MOVWF	FSR0H -	;
	BSF	EECON1, EEPGD	; Point to program memory
	BCF	EECON1,CFGS	; Not configuration space
	BSF	EECON1,WREN	; Enable writes
	BSF	EECON1, LWLO	; Only Load Write Latches
LOOP			
	MOVIW	FSR0++	; Load first data byte into lower
	MOVWF	EEDATL	;
	MOVIW	FSR0++	; Load second data byte into upper
	MOVWF	EEDATH	;
	MOVF	EEADRL,W	; Check if lower bits of address are '000'
	XORLW	0x07	; Check if we're on the last of 8 addresses
	ANDLW	0x07	;
	BTFSC	STATUS,Z	; Exit if last of eight words,
	GOTO	START_WRITE	;
	MOVLW	55h	; Start of required write sequence:
	MOVWF	EECON2	; Write 55h
	MOVLW	0AAh	, WIICE JJH
ed	MOVWF		, Write AAh
Required Sequence	BSF		; Set WR bit to begin write
Sec	NOP	2200117,111	; Any instructions here are ignored as processor
- 0			; halts to begin write sequence
	NOP		; Processor will stop here and wait for write to complete.
			· <u>·</u> <u>·</u>
			; After write processor continues with 3rd instruction.
	INCF	EEADRL,F	; Still loading latches Increment address
	GOTO	LOOP	; Write next latches
START_V	WRITE		
	BCF	EECON1,LWLO	; No more loading latches - Actually start Flash program
			; memory write
	MOVLW	55h	; Start of required write sequence:
0	MOVWF	EECON2	; Write 55h
Required Sequence	MOVLW	0AAh	;
quii	MOVWF	EECON2	; Write AAh
Sec Sec	BSF	EECON1,WR	; Set WR bit to begin write
	NOP		; Any instructions here are ignored as processor
	NOD		; halts to begin write sequence
	NOP		; Processor will stop here and wait for write complete.
			; after write processor continues with 3rd instruction
	BCF	EECON1,WREN	; Disable writes
	BSF	INTCON, GIE	; Enable interrupts
		,011	,,, ,,,,,,,,,,,,,

11.4 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

- 1. Load the starting address of the row to be modified.
- 2. Read the existing data from the row into a RAM image.
- 3. Modify the RAM image to contain the new data to be written into program memory.
- 4. Load the starting address of the row to be rewritten.
- 5. Erase the program memory row.
- 6. Load the write latches with data from the RAM image.
- 7. Initiate a programming operation.
- 8. Repeat steps 6 and 7 as many times as required to reprogram the erased row.

11.5 User ID, Device ID and Configuration Word Access

Instead of accessing program memory or EEPROM data memory, the User ID's, Device ID/Revision ID and Configuration Words can be accessed when CFGS = 1 in the EECON1 register. This is the region that would be pointed to by PC<15> = 1, but not all addresses are accessible. Different access may exist for reads and writes. Refer to Table 11-2.

When read access is initiated on an address outside the parameters listed in Table 11-2, the EEDATH:EEDATL register pair is cleared.

Address	Function	Read Access	Write Access
8000h-8003h	User IDs	Yes	Yes
8006h	Device ID/Revision ID	Yes	No
8007h-8008h	Configuration Words 1 and 2	Yes	No

TABLE 11-2: USER ID, DEVICE ID AND CONFIGURATION WORD ACCESS (CFGS = 1)

EXAMPLE 11-3: CONFIGURATION WORD AND DEVICE ID ACCESS

 * This code block will read 1 word of program memory at the memory address: PROG ADDR LO (must be 00h-08h) data will be returned in the variables; PROG DATA HI, PROG DATA LO BANKSEL EEADRL ; Select correct Bank ; MOVLW PROG ADDR LO ; Store LSB of address MOVWF EEADRL CLRF EEADRH ; Clear MSB of address EECON1,CFGS ; Select Configuration Space BSF INTCON,GIE BCF ; Disable interrupts EECON1,RD ; Initiate read BSF ; Executed (See Figure 11-1) NOP NOP ; Ignored (See Figure 11-1) INTCON,GIE BSF ; Restore interrupts MOVE EEDATL,W ; Get LSB of word PROG DATA LO ; Store in user location MOVWF MOVE EEDATH,W ; Get MSB of word MOVWF PROG DATA HI ; Store in user location

11.6 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM or program memory should be verified (see Example 11-6) to the desired value to be written. Example 11-6 shows how to verify a write to EEPROM.

EXAMPLE 11-6: EEPROM WRITE VERIFY

BANKSEI	L EEDATL		;
MOVF	EEDATL,	W	;EEDATL not changed
			;from previous write
BSF	EECON1,	RD	;YES, Read the
			;value written
XORWF	EEDATL,	W	;
BTFSS	STATUS,	Ζ	;Is data the same
GOTO	WRITE_E	RR	;No, handle error
:			;Yes, continue

REGISTER 11-1: EEDATL: EEPROM DATA REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
			EEDA	\T<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit	t	W = Writable bit		U = Unimpleme	ented bit, read as	'0'	
u = Bit is unchan	ged	x = Bit is unknov	vn	-n/n = Value at	POR and BOR/V	alue at all other f	Resets
'1' = Bit is set		'0' = Bit is cleare	d				

bit 7-0

EEDAT<7:0>: Read/write value for EEPROM data byte or Least Significant bits of program memory

REGISTER 11-2: EEDATH: EEPROM DATA HIGH BYTE REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u		
—	—		EEDAT<13:8>						
bit 7							bit 0		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 Unimplemented: Read as '0'

bit 5-0 EEDAT<13:8>: Read/write value for Most Significant bits of program memory

REGISTER 11-3: EEADRL: EEPROM ADDRESS REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
			EEAD	R<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit		W = Writable bit		U = Unimplemented bit, read as '0'				
u = Bit is unchang	ged	x = Bit is unknown	t is unknown -n/n = Value at POR and BOR/Value at all other Resets					

bit 7-0 EEADR<7:0>: Specifies the Least Significant bits for program memory address or EEPROM address

REGISTER 11-4: EEADRH: EEPROM ADDRESS HIGH BYTE REGISTER

'0' = Bit is cleared

U-1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—				EEADR<14:8>	>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 Unimplemented: Read as '0'

bit 6-0 EEADR<14:8>: Specifies the Most Significant bits for program memory address or EEPROM address

'1' = Bit is set

R/W-0/0	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W-x/q	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0		
EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD		
bit 7							bit C		
Legend:									
R = Readable		W = Writable			nented bit, rea				
S = Bit can on	•	x = Bit is unk				R/Value at all o	ther Resets		
'1' = Bit is set		'0' = Bit is cle	ared	HC = Bit is cl	eared by hardv	vare			
bit 7	EEPGD: Flas	sh Program/Da	ta EEPROM M	emorv Select	bit				
		•	ce Flash memo	•					
	0 = Accesse	s data EEPRC	M memory						
bit 6	CFGS: Flash	Program/Data	EEPROM or C	Configuration S	Select bit				
		•	n, User ID and I	-					
		-	m or data EEP	ROM Memory					
bit 5		Write Latches	•						
			<u>space)</u> OR <u>CF(</u>				n latabaa ar		
		ated.	nmand does no	ot initiate a w	nte; only the p	program memor	y latches an		
			mand writes a v	alue from EEI	DATH:EEDATL	into program m	emory latche		
	and	initiates a writ	e of all the data	stored in the	program memo	ory latches.			
	If CEGS = 0 a	and FFPGD =	0: (Accessing o	lata FFPROM					
			WR command i			EPROM.			
bit 4	FREE: Progr	am Flash Eras	e Enable bit						
	<u>If CFGS = 1</u>	(Configuration	<u>space)</u> OR <u>CFC</u>	<u>GS = 0</u> and EE	<u>EPGD = 1 (prog</u>	<u>gram Flash)</u> :			
			operation on the	he next WR co	ommand (clear	ed by hardware	after comple		
		of erase).	peration on the	novt W/D com	mand				
		ionns a white o			inanu.				
			<u>0:</u> (Accessing						
	-			will initiate bot	h a erase cycle	e and a write cyo	de.		
bit 3		PROM Error F	0						
	1 = Condition indicates an improper program or erase sequence attempt or termination (bit is set automatically on any set attempt (write '1') of the WR bit).								
bit 2	 0 = The program or erase operation completed normally. WREN: Program/Erase Enable bit 								
	-	rogram/erase							
	0 = Inhibits p	programming/e	rasing of progra	am Flash and	data EEPROM	l			
bit 1	WR: Write Co	ontrol bit							
			sh or data EEPI						
						operation is co	mplete.		
		•	e set (not cleare on to the Flash	,		e and inactive			
bit 0	RD: Read Co	-							
	1 = Initiates		lash or data F	FPROM read	. Read takes	one cycle RD	is cleared in		
		an program F	Flash or data E an only be set			one cycle. RD	is cleared in		

REGISTER 11-5: EECON1: EEPROM CONTROL 1 REGISTER

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
		l	EEPROM Co	ontrol Register 2			
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable bit		U = Unimplemented bit, read as '0'			
S = Bit can only b	oe set	x = Bit is unknown		-n/n = Value at POR and BOR/Value at all othe			ther Resets
'1' = Bit is set		'0' = Bit is clea	ared				

bit 7-0 Data EEPROM Unlock Pattern bits

To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the EECON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes. Refer to **Section 11.2.2** "Writing to the Data EEPROM Memory" for more information.

TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
EECON1	EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	121
EECON2	2 EEPROM Control Register 2 (not a physical register)								
EEADRL	EEADRL<7:0>								120
EEADRH	EEADRH<6:0								120
EEDATL	EEDATL<7:0>								120
EEDATH	_	—			EEDAT	H<5:0>			120
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	95
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	99

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by data EEPROM module.

* Page provides register information.

12.0 I/O PORTS

Depending on the device selected and peripherals enabled, there are up to two ports available. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has three standard registers for its operation. These registers are:

- TRISx registers (data direction)
- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)

Some ports may have one or more of the following additional registers. These registers are:

- ANSELx (analog select)
- WPUx (weak pull-up)
- INLVLx (input level control)

TABLE 12-1:PORT AVAILABILITY PER
DEVICE

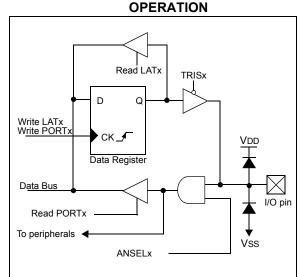
Device	PORTA	PORTB	PORTC
PIC16F/LF1825	•		•
PIC16F/LF1829	•	•	•

The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same affect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports with analog functions also have an ANSELx register which can disable the digital input and save power. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 12-1.

FIGURE 12-1: GENERIC I/O PORT



12.1 Alternate Pin Function

The Alternate Pin Function Control 0 (APFCON0) and Alternate Pin Function Control 1 (APFCON1) registers are used to steer specific peripheral input and output functions between different pins. The APFCON0 and APFCON1 registers are shown in Register 12-1 and Register 12-2. For this device family, the following functions can be moved between different pins.

- RX/DT/TX/CK
- SDO
- SS (Slave Select)
- T1G
- P1B/P1C/P1D/P2B
- CCP1/P1A/CCP2

These bits have no effect on the values of any TRIS register. PORT and TRIS overrides will be routed to the correct pin. The unselected pin will be unaffected.

REGISTER 12-1: APFCON0: ALTERNATE PIN FUNCTION CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	U-0	U-0
RXDTSEL	SDOSEL	SSSEL	_	T1GSEL	TXCKSEL	_	_
bit 7							bit
Legend: R = Readable I	hit	W = Writable bit		U = Unimplem	ented bit, read as	ʻ0'	
u = Bit is uncha		x = Bit is unknow			POR and BOR/Va		Resets
'1' = Bit is set		'0' = Bit is cleare					
bit 7	0 = RX/DT f 1 = RX/DT f For 20 Pin De 0 = RX/DT f	n Selection bit vices (PIC16F/LF1 unction is on RC5 unction is on RA1 vices (PIC16F/LF1 unction is on RB5 unction is on RC5	-				
bit 6	0 = SDO fur 1 = SDO fur <u>For 20 Pin De</u> Bit is read-only	vices (PIC16F/LF1 nction is on RC2 nction is on RA4 vices (PIC16F/LF1	·				
bit 5	$0 = \frac{SS1}{SS1} \text{ fun}$ 1 = SS1 fun For 20 Pin De Bit is read-only	<u>vices (</u> PIC16F/LF1 ction is on RC3 ction is on RA3 <u>vices (</u> PIC16F/LF1	829 <u>)</u> :				
bit 4	Unimplement	ed: Read as '0'					
bit 3		Selection bit ction is on RA4 ction is on RA3					
bit 2	0 = TX/CK f 1 = TX/CK f <u>For 20 Pin De</u> 0 = TX/CK f	n Selection bit <u>vices (</u> PIC16F/LF1 unction is on RC4 unction is on RA0 <u>vices (</u> PIC16F/LF1 unction is on RB7 unction is on RC4	-				

REGISTER 12-2:	APFCON1: ALTERNATE PIN FUNCTION CONTROL REGISTER 1
----------------	--

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
_	_	SDO2SEL ⁽¹⁾	SS2SEL ⁽¹⁾	P1DSEL	P1CSEL	P2BSEL	CCP2SEL
bit 7	•					•	bit C
Legend:							
R = Readable	bit	W = Writable bit	t	U = Unimpleme	nted bit, read as	'0'	
u = Bit is unch	nanged	x = Bit is unknow	wn	-n/n = Value at	POR and BOR/V	alue at all other l	Resets
'1' = Bit is set		'0' = Bit is cleare	ed				
bit 7-6	Unimplemen	ted: Read as '0'					
bit 5	SDO2SEL: P	in Selection bit ⁽¹⁾					
		function is on RC1					
		function is on RA5					
bit 4		Selection bit ⁽¹⁾					
		nction is on RC0					
		nction is on RA4					
bit 3	P1DSEL: Pin						
	• • • • • • • •	nction is on RC2					
hit 0							
bit 2	P1CSEL: Pin 0 = P1C fui	nction is on RC3					
		nction is on RC3					
bit 1	P2BSEL: Pin						
		nction is on RC2					
	1 = P2B fur	nction is on RA4					
bit 0	CCP2SEL: P	in Selection bit					
	0 = CCP2 f	unction is on RC3					
	1 = CCP2 f	unction is on RA5					

Note 1: PIC16F/LF1829 only.

12.2 PORTA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 12-4). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '1'. Example 12-1 shows how to initialize PORTA.

Reading the PORTA register (Register 12-3) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATA).

The TRISA register (Register 12-4) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

The INLVLA register (Register 12-8) controls the input voltage threshold for each of the available PORTA input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTA register and also the level at which an Interrupt-on-Change occurs, if that feature is enabled. See Section 30.4 "DC Characteristics: PIC16F/LF1825/1829-I/E" for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

12.2.1 ANSELA REGISTER

The ANSELA register (Register 12-6) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA register must be initialized						
	to configure an analog channel as a digital						
	input. Pins configured as analog inputs						
	will read '0'.						

EXAMPLE 12-1: INITIALIZING PORTA

BANKSEL	PORTA	;
CLRF	PORTA	;Init PORTA
BANKSEL	LATA	;Data Latch
CLRF	LATA	;
BANKSEL	ANSELA	;
CLRF	ANSELA	;digital I/O
BANKSEL	TRISA	;
MOVLW	B'00111000'	;Set RA<5:3> as inputs
MOVWF	TRISA	;and set RA<2:0> as
		;outputs

12.2.2 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions. The pins, their combined functions and their output priorities are briefly described here. For additional information, refer to the appropriate section in this data sheet.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the lowest number in the following lists.

Analog input functions, such as ADC, comparator and Cap Sense inputs, are not shown in the priority lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx registers. Digital output functions may control the pin when it is in Analog mode with the priority shown below.

<u>RA0</u>

- 1. ICSPDAT
- 2. ICDDAT
- 3. DACOUT (DAC)

<u>RA1</u>

- 1. ICSPCLK
- 2. ICDCLK
- 3. RX/DT (EUSART)

<u>RA2</u>

- 1. SRQ
- 2. C1OUT (Comparator)
- 3. CCP3

<u>RA3</u>

No output priorities. Input only pin.

<u>RA4</u>

- 1. CLKOUT
- 2. T10SO
- 3. CLKR
- 4. SDO
- 5. P2B

<u>RA5</u>

- 1. SDO2 (MSSP) (PIC16F/LF1829 only)
- 2. CCP2/P2A

U-0	U-0	R/W-x/x	R/W-x/x	R-x/x	R/W-x/x	R/W-x/x	R/W-x/x		
	_	RA5	RA4	RA3	RA2	RA1	RA0		
bit 7		•		·			bit 0		
Legend:									
R = Readable bit W = Wr		W = Writable	N = Writable bit		U = Unimplemented bit, read as '0'				
u = Bit is unchanged		x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets		
'1' = Bit is set		'0' = Bit is cle	ared						
bit 7-6	Unimplemer	ted: Read as '	0'						

REGISTER 12-3: PORTA: PORTA REGISTER

bit 7-6	Unimplemented: Read as '0'
bit 5-0	RA<5:0>: PORTA I/O Value bits ⁽¹⁾
	1 = Port pin is <u>></u> V ін
	0 = Port pin is <u><</u> VIL

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 12-4: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R-1/1	R/W-1/1	R/W-1/1	R/W-1/1
_	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0'
bit 5-4	TRISA<5:4>: PORTA Tri-State Control bit 1 = PORTA pin configured as an input (tri-stated) 0 = PORTA pin configured as an output
bit 3	TRISA3: RA3 Port Tri-State Control bit This bit is always '1' as RA3 is an input only
bit 2-0	TRISA<2:0>: PORTA Tri-State Control bit 1 = PORTA pin configured as an input (tri-stated) 0 = PORTA pin configured as an output

U-0	U-0	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
u = Bit is unchanged x = Bit is unknown		-n/n = Value at POR and BOR/Value at all other Resets					
'1' = Bit is set		'0' = Bit is clea	ared				

REGISTER 12-5: LATA: PORTA DATA LATCH REGISTER

bit 7-6	Unimplemented: Read as '0'
bit 5-4	LATA<5:4>: RA<5:4> Output Latch Value bits ⁽¹⁾
bit 3	Unimplemented: Read as '0'

bit 2-0 LATA<2:0>: RA<2:0> Output Latch Value bits⁽¹⁾

REGISTER 12-6: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	U-0	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5	Unimplemented: Read as '0'
bit 4	 ANSA4: Analog Select between Analog or Digital Function on pins RA4, respectively 0 = Digital I/O. Pin is assigned to port or digital special function. 1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.
bit 3	Unimplemented: Read as '0'
bit 2-0	 ANSA<2:0>: Analog Select between Analog or Digital Function on pins RA<2:0>, respectively 0 = Digital I/O. Pin is assigned to port or digital special function. 1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.
Note 1:	When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	
—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	
bit 7							bit 0	
Legend:								
R = Readable b	oit	W = Writable	bit	U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unknown		own	-n/n = Value at POR and BOR/Value at all other Resets					
'1' = Bit is set '0' = Bit is cleared			ared					
L								

REGISTER 12-7: WPUA: WEAK PULL-UP PORTA REGISTER

bit 7-6	Unimplemented: Read as '0'
bit 5-0	WPUA<5:0>: Weak Pull-up Register bits
	1 = Pull-up enabled
	0 = Pull-up disabled

Note 1: Global WPUEN bit of the OPTION register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

REGISTER 12-8: INLVLA: PORTA INPUT LEVEL CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-0/0
—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0'

bit 5-0 INLVLA<5:0>: PORTA Input Level Select bits For RA<5:0> pins, respectively 1 = ST input used for port reads and interrupt-on-change 0 = TTL input used for port reads and interrupt-on-change

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TABLE 12-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	130
APFCON0	RXDTSEL	SDOSEL ⁽²⁾	SSSEL ⁽²⁾	_	T1GSEL	TXCKSEL	_	_	125
APFCON1	_	_	SDO2SEL ⁽¹⁾	SS2SEL ⁽¹⁾	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	126
INLVLA	_	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
LATA	_	_	LATA5	LATA4	_	LATA2	LATA1	LATA0	130
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA		PS<2:0>		189
PORTA	_	—	RA5	RA4	RA3	RA2	RA1	RA0	129
TRISA	_	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
WPUA	—	_	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	131

Legend:

x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1:

PIC16F/LF1829 only. PIC16F/LF1825 only. 2:

SUMMARY OF CONFIGURATION WORD WITH PORTA **TABLE 12-3**:

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
0015104	13:8	_		FCMEN	IESO	CLKOUTEN	BORE	N<1:0>	CPD	50
CONFIG1	7:0	CP	MCLRE	PWRTE	WDTE<1:0>		FOSC<2:0>			52

Legend: - = unimplemented location, read as '0'. Shaded cells are not used by PORTA.

Note 1: PIC16F1825/1829 only.

12.3 PORTB Registers (PIC16F/LF1829 only)

PORTB is a 4-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 12-10). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 12-2 shows how to initialize PORTB.

Reading the PORTB register (Register 12-9) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATB).

The TRISB register (Register 12-10) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

The INLVLB register (Register 12-14) controls the input voltage threshold for each of the available PORTB input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTB register and also the level at which an Interrupt-on-Change occurs, if that feature is enabled. See Section 30.4 "DC Characteristics: PIC16F/LF1825/1829-I/E" for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

12.3.1 ANSELB REGISTER

The ANSELB register (Register 12-12) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELB bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no affect on digital output functions. A pin with TRIS clear and ANSELB set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELB register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 12-2: INITIALIZING PORTB

BANKSEL	PORTB	;
CLRF	PORTB	;Init PORTB
BANKSEL	LATB	;Data Latch
CLRF	LATB	;
BANKSEL	ANSELB	
CLRF	ANSELB	;Make RB<7:4> digital
BANKSEL	TRISB	;
MOVLW	B'00110000'	;Set RB<5:4> as inputs
		;and RB<3:0> as outputs
MOVWF	TRISB	;

12.3.2 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTB pin is multiplexed with other functions. The pins, their combined functions and their output priorities are briefly described here. For additional information, refer to the appropriate section in this data sheet.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the lowest number in the following lists.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

RB4

1. SDA (MSSP)

<u>RB5</u>

- 1. SDA2 (MSSP) (PIC16F1829 only)
- 2. RX/DT (EUSART)

<u>RB6</u>

1. SCL/SCK (MSSP)

<u>RB7</u>

1. TX/CK (EUSART)

REGISTER 12-9: PORTB: PORTB REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0
RB7	RB6	RB5	RB4	_	—	—	_
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	V = Writable bit		U = Unimplemented bit, read as '0'		
u = Bit is unchanged x = Bit is unknown		nown	-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set '0' = Bit is cleared							

bit 7-4	RB<7:4>: PORTB General Purpose I/O Pin bits
	1 = Port pin is <u>></u> Vін
	0 = Port pin is <u><</u> VIL
bit 3-0	Unimplemented: Read as '0'

REGISTER 12-10: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
TRISB7	TRISB6	TRISB5	TRISB4	_	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **TRISB<7:4>:** PORTB Tri-State Control bits 1 = PORTB pin configured as an input (tri-stated) 0 = PORTB pin configured as an output

bit 3-0 Unimplemented: Read as '0'

REGISTER 12-11: LATB: PORTB DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0
LATB7	LATB6	LATB5	LATB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 3-0 Unimplemented: Read as '0'

Note 1: Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

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REGISTER 12-12: ANSELB: PORTB ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0			
ANSB7	ANSB6	ANSB5	ANSB4	—			_			
bit 7							bit (
Legend:										
R = Readable bi	t	W = Writable bi	t	U = Unimplemented bit, read as '0'						
u = Bit is unchar	nged	x = Bit is unkno	wn	-n/n = Value at I	POR and BOR/V	alue at all other	Resets			
'1' = Bit is set		'0' = Bit is clear	ed							

Digital I/O. Pin is assigned to port or digital special function.
 Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

bit 3-0 Unimplemented: Read as '0'

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 12-13: WPUB: WEAK PULL-UP PORTB REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
WPUB7	WPUB6	WPUB5	WPUB4	—			—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 WPUB<7:4>: Weak Pull-up Register bits 1 = Pull-up enabled 0 = Pull-up disabled bit 3-0 Unimplemented: Read as '0'

Note 1: Global WPUEN bit of the OPTION register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

REGISTER 12-14: INLVLB: PORTB INPUT LEVEL CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0			
INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—			
bit 7							bit 0			
Legend:										
R = Readable bit		W = Writable bi	t	U = Unimplemented bit, read as '0'						
u = Bit is unchan	u = Bit is unchanged x = Bit is unknown				-n/n = Value at POR and BOR/Value at all other Resets					
'1' = Bit is set		'0' = Bit is clear	ed							
bit 7-4	INLVLB<7:4>:	PORTB Input Le	vel Select bits							
	For RB<7:4> pi	ns, respectively								
	1 = ST input us	ed for PORT rea	ds and Interrup	t-on-Change						
	0 = TTL input u	sed for PORT re	ads and Interru	pt-on-Change						
bit 7-6	Unimplemente	d: Read as '0'								
	-									

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	_	—	—	—	136
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	_	—	—	—	136
LATB	LATB7	LATB6	LATB5	LATB4	_	—	—	—	135
PORTB	RB7	RB6	RB5	RB4	_	_	_	_	135
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	_	—	—	—	135
WPUB	WPUB7	WPUB6	WPUB5	WPUB4		—	_	_	136

TABLE 12-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB⁽¹⁾

 Legend:
 x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

 Note
 1:
 PIC16F/LF1829 only.

12.4 PORTC Registers

PORTC is a 6-bit wide (8-bit wide for PIC16F/LF1829), bidirectional port. The corresponding data direction register is TRISC (Register 12-10). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 12-2 shows how to initialize PORTC.

Reading the PORTC register (Register 12-9) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATC).

The TRISC register (Register 12-10) controls the PORTC pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

The INLVLC register (Register 12-20) controls the input voltage threshold for each of the available PORTC input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTC register and also the level at which an Interrupt-on-Change occurs, if that feature is enabled. See Section 30.4 "DC Character-istics: PIC16F/LF1825/1829-I/E" for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

12.4.1 ANSELC REGISTER

The ANSELC register (Register 12-12) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELC bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELC bits has no affect on digital output functions. A pin with TRIS clear and ANSELC set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELC register must be initialized									
	to configure an analog channel as a digital									
	input. Pins configured as analog inputs									
	will read '0'.									

EXAMPLE 12-3: INITIALIZING PORTC

BANKSEL	PORTC	;
CLRF	PORTC	;Init PORTC
BANKSEL	LATC	;Data Latch
CLRF	LATC	;
BANKSEL	ANSELC	
CLRF	ANSELC	;Make RC<5:0> digital
BANKSEL	TRISC	;
MOVLW	B'00110000'	;Set RC<5:4> as inputs
		;and RC<3:0> as outputs
MOVWF	TRISC	;

12.4.2 PORTC FUNCTIONS AND OUTPUT PRIORITIES

Each PORTC pin is multiplexed with other functions. The pins, their combined functions and their output priorities are briefly described here. For additional information, refer to the appropriate section in this data sheet.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the lowest number in the following lists.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

<u>RC0</u>

- 1. SCL (MSSP) (PIC16F/LF1825 only)
- 2. SCK (MSSP) (PIC16F/LF1825 only)
- 3. P1D

<u>RC1</u>

- 1. SDA1 (MSSP) (PIC16F/LF1825 only)
- 1. SDA1 (MSSP) (PIC16F/LF1829 only)
- 2. P1C

<u>RC2</u>

- 1. SDO (MSSP) (PIC16F/LF1825 only)
- 2. P1D
- 3. P2B

<u>RC3</u>

- 1. SS1 (MSSP) (PIC16F/LF1825 only)
- 2. CCP2
- 3. P1C
- 4. P2A

<u>RC4</u>

- 1. MDOUT
- 2. SRNQ
- 3. C2OUT
- 4. TX/CK
- 5. P1B

<u>RC5</u>

- 1. RX/DT
- 2. CCP1/P1A

RC6 (PIC16F/LF1829 only)

- 1. SS1 (MSSP)
- 2. CCP4
- RC7 (PIC16F/LF1829 only)
- 1. SDO (MSSP)

REGISTER 12-15: PORTC: PORTC REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	
RC7 ⁽¹⁾	RC6 ⁽¹⁾	RC5	RC4	RC3	RC2	RC1	RC0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unknown			nown	-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set		'0' = Bit is clea	ared					

bit 7-0 RC<7:0>: PORTC General Purpose I/O Pin bits⁽¹⁾ 1 = Port pin is ≥ VIH 0 = Port pin is ≤ VIL

Note 1: RC<7:6> available on PIC16F/LF1829 only. Otherwise, they are unimplemented and read as '0'.

REGISTER 12-16: TRISC: PORTC TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7				•			bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 TRISC<7:0>: PORTC Tri-State Control bits⁽¹⁾

1 = PORTC pin configured as an input (tri-stated)

0 = PORTC pin configured as an output

Note 1: TRISC<7:6> available on PIC16F/LF1829 only. Otherwise, they are unimplemented and read as '0'.

REGISTER 12-17: LATC: PORTC DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATC7 ⁽²⁾	LATC6 ⁽²⁾	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 LATC<7:0>: PORTC Output Latch Value bits^(1, 2)

- **Note 1:** Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register is return of actual I/O pin values.
 - 2: LATC<7:6> available on PIC16F/LF1829 only. Otherwise, they are unimplemented and read as '0'.

R/W-1/1	R/W-1/1	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1				
ANSC7 ⁽²⁾	ANSC6 ⁽²⁾		_	ANSC3	ANSC2	ANSC1	ANSC0				
bit 7				•			bit 0				
Legend:											
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'					
u = Bit is und	hanged	x = Bit is unkn	own	-n/n = Value at POR and BOR/Value at all other Res							
'1' = Bit is se	t	'0' = Bit is clea	ared								
bit 7-6	0 = Digital I/	: Analog Select ′O. Pin is assign input. Pin is ass	ed to port or o	digital special fu	inction.		ectively ⁽²⁾				
bit 5-4	Unimplemer	nted: Read as '	כ'								
bit 3-0	0 = Digital I/	 Unimplemented: Read as '0' ANSC<3:0>: Analog Select between Analog or Digital Function on pins RC<3:0>, respectively 0 = Digital I/O. Pin is assigned to port or digital special function. 1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled. 									

REGISTER 12-18: ANSELC: PORTC ANALOG SELECT REGISTER

- **Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.
 - 2: ANSELC<7:6> available on PIC16F/LF1829 only. Otherwise, they are unimplemented and read as '0'.

REGISTER 12-19: WPUC: WEAK PULL-UP PORTC REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
WPUC7 ⁽³⁾	WPUC6 ⁽³⁾	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7	<u>.</u>						bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 WPUC<7:0>: Weak Pull-up Register bits^(1, 2) 1 = Pull-up enabled 0 = Pull-up disabled

Note 1: Global WPUEN bit of the OPTION register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

3: WPUC<7:6> available on PIC16F/LF1829 only. Otherwise, they are unimplemented and read as '0'.

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							1
R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-0/0
INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
bit 7							bit 0
Legend:							
R = Readable b	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
u = Bit is uncha	= Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Valu			R/Value at all o	ther Resets		
'1' = Bit is set		'0' = Bit is clea	ared				

REGISTER 12-20: INLVLC: PORTC INPUT LEVEL CONTROL REGISTER

bit 7-0 INLVLC<7:0>: PORTC Input Level Select bits⁽¹⁾ For RC<7:0> pins, respectively 1 = ST input used for port reads and interrupt-on-change 0 = TTL input used for port reads and interrupt-on-change

Note 1: INLVLC<7:6> available on PIC16F/LF1829 only. Otherwise, they are unimplemented and read as '0'.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELC	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	_	_	ANSC3	ANSC2	ANSC1	ANSC0	136
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
LATC	LATC7 ⁽¹⁾	LATC6 ⁽¹⁾	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	135
PORTC	RC7 ⁽¹⁾	RC6 ⁽¹⁾	RC5	RC4	RC3	RC2	RC1	RC0	135
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	135
WPUC	WPUC7 ⁽¹⁾	WPUC6 ⁽¹⁾	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	136

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

Note 1: PIC16F/LF1829 only.

2: PIC16F/LF1825 only.

13.0 INTERRUPT-ON-CHANGE

The PORTA pins can be configured to operate as Interrupt-On-Change (IOC) pins. On the PIC16F/LF1829 devices, the PORTB pins can also be configured to operate as IOC pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual port pin, or combination of port pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- · Rising and falling edge detection
- · Individual pin interrupt flags

Figure 13-1 is a block diagram of the IOC module.

13.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

13.2 Individual Pin Configuration

For each port pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both associated bits of the IOCxP and IOCxN registers, respectively.

13.3 Interrupt Flags

The IOCAFx and IOCBFx bits located in the IOCAF and IOCBF registers, respectively, are status flags that correspond to the Interrupt-on-change pins of the associated port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCAFx and IOCBFx bits.

13.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx and IOCBFx bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 13-1:

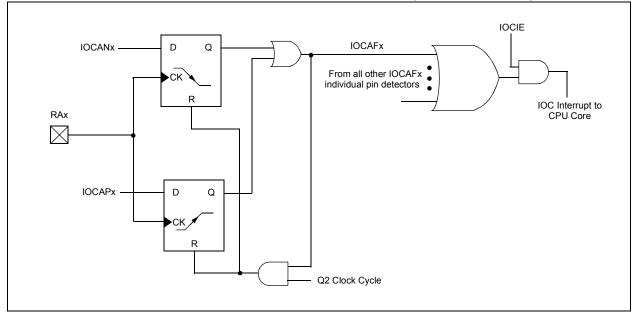
MOVLW 0xff XORWF IOCAF, W ANDWF IOCAF, F

13.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCxF register will be updated prior to the first instruction executed out of Sleep.

FIGURE 13-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM (PORTA EXAMPLE)



REGISTER 13-1: IOCAP: INTERRUPT-ON-CHANGE PORTA POSITIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
bit 7	·	·				•	bit 0
Legend:							
R = Readable b	bit	W = Writable b	oit	U = Unimplem	ented bit, read a	as 'O'	
u = Bit is uncha	anged	x = Bit is unkne	own	-n/n = Value at POR and BOR/Value at all other Rese			er Resets
'1' = Bit is set		'0' = Bit is clea	red				

bit 7-6	Unimplemented:	Read	as	'0'

bit 5-0 IOCAP<5:0>: Interrupt-on-Change PORTA Positive Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-2: IOCAN: INTERRUPT-ON-CHANGE PORTA NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 Unimplemented: Read as '0'

bit 5-0

IOCAN<5:0>: Interrupt-on-Change PORTA Negative Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **IOCAF<5:0>:** Interrupt-on-Change PORTA Flag bits

1 = An enabled change was detected on the associated pin.

Set when IOCAPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RAx.

0 = No change was detected, or the user cleared the detected change.

REGISTER 13-4: IOCBP: INTERRUPT-ON-CHANGE PORTB POSITIVE EDGE REGISTER (PIC16F/LF1829 ONLY)

Legend: R = Readable b							
bit 7							bit 0
IOCBP7	IOCBP6	IOCBP5	IOCBP4	—		—	—
R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0

R = Readable bit	VV = VVritable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4	IOCBP<7:4>: Interrupt-on-Change PORTB Positive Edge Enable bits
	1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt
	flag will be set upon detecting an edge.
	0 = Interrupt-on-Change disabled for the associated pin.
bit 3-0	Unimplemented: Read as '0'

REGISTER 13-5: IOCBN: INTERRUPT-ON-CHANGE PORTB NEGATIVE EDGE REGISTER (PIC16F/LF1829 ONLY)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
IOCBN7	IOCBN6	IOCBN5	IOCBN4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4	IOCAN<7:4>: Interrupt-on-Change PORTB Negative Edge Enable bits
	1 = Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt
	flag will be set upon detecting an edge.
	0 = Interrupt-on-Change disabled for the associated pin.
bit 5-0	Unimplemented: Read as '0'

REGISTER 13-6: IOCBF: INTERRUPT-ON-CHANGE PORTB FLAG REGISTER (PIC16F/LF1829 ONLY)

'0' = Bit is cleared

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	
IOCBF7	IOCBF6	IOCBF5	IOCBF4	—	—	—	_	
bit 7	•	•					bit 0	
Legend:								
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'					
u = Bit is unchanged x = Bit is unknown		-n/n = Value at POR and BOR/Value at all other Resets						

HS - Bit is set in hardware

bit 7-4	 IOCBF<7:4>: Interrupt-on-Change PORTB Flag bits 1 = An enabled change was detected on the associated pin. Set when IOCBPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RBx. 0 = No change was detected, or the user cleared the detected change.
bit 5-0	Unimplemented: Read as '0'

TABLE 13-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	_	ANSA4	—	ANSA2	ANSA1	ANSA0	130
ANSELB ⁽¹⁾	ANSB7	ANSB6	ANSB5	ANSB4	—	—	_	—	136
INLVLA	—	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	_	—	136
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
IOCAF	_	_	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	144
IOCAN	—	_	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	144
IOCAP	—	_	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	144
IOCBF ⁽¹⁾	IOCBF7	IOCBF6	IOCBF5	IOCBF4			_		146
IOCBN ⁽¹⁾	IOCBN7	IOCBN6	IOCBN5	IOCBN4	_	_	_	_	145
IOCBP ⁽¹⁾	IOCBP7	IOCBP6	IOCBP5	IOCBP4	—	—	—	—	145
TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	_	_		_	135

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Interrupt-on-Change.

Note 1: PIC16F/LF1829 only.

'1' = Bit is set

14.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference, or FVR, is a stable voltage reference, independent of VDD, with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

- · ADC input channel
- · ADC positive reference
- · Comparator positive input
- Digital-to-Analog Converter (DAC)

The FVR can be enabled by setting the FVREN bit of the FVRCON register.

14.1 Independent Gain Amplifiers

The output of the FVR supplied to the ADC, Comparators, and DAC is routed through two independent programmable gain amplifiers. Each amplifier can be configured to amplify the reference voltage by 1x, 2x or 4x, to produce the three possible voltage levels.

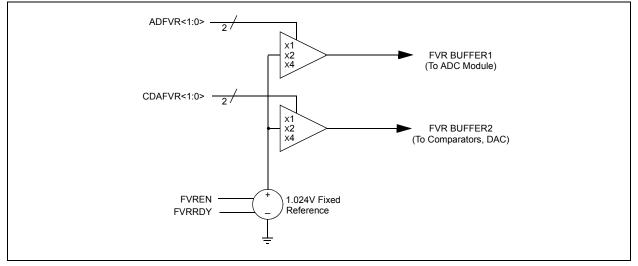
The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference **Section 16.0** "**Analog-to-Digital Converter** (**ADC**) **Module**" for additional information.

The CDAFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the DAC and comparator module. Reference Section 17.0 "Digital-to-Analog Converter (DAC) Module" and Section 19.0 "Comparator Module" for additional information.

14.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the FVRRDY bit of the FVRCON register will be set. See **Section 30.0** "**Electrical Specifications**" for the minimum delay requirement.

FIGURE 14-1: VOLTAGE REFERENCE BLOCK DIAGRAM



R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVREN	FVRRDY ⁽¹⁾	TSEN	TSRNG	CDAFVR1	CDAFVR0	ADFVR1	ADFVR0
bit 7							bit
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
u = Bit is unc	hanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BOI	R/Value at all c	ther Resets
'1' = Bit is set	•	'0' = Bit is cle	ared	q = Value dep	pends on conditi	on	
bit 7	0 = Fixed Vo	d Voltage Refe tage Referenc tage Referenc	e is disabled	bit			
bit 6	0 = Fixed Vo	ed Voltage Rei tage Referenc tage Referenc	e output is no	t ready or not e	enabled		
bit 5	0 = Tempera	erature Indicator ture Indicator is ture Indicator is	s disabled				
bit 4	0 = VOUT = V	perature Indica DD - 4VT (High DD - 2VT (Low	Range)	election bit			
bit 3-2	CDAFVR<1:0 00 = Compara 01 = Compara 10 = Compara	I>: Comparato ator and DAC I ator and DAC I ator and DAC I	r and DAC Fix Fixed Voltage Fixed Voltage Fixed Voltage	Reference Per Reference Per Reference Per	ference Selectic ipheral output is ipheral output is ipheral output is ipheral output is	s off s 1x (1.024V) s 2x (2.048V) ⁽²	
bit 1-0	 11 = Comparator and DAC Fixed Voltage Reference Peripheral output is 4x (4.096V)⁽²⁾ ADFVR<1:0>: ADC Fixed Voltage Reference Selection bit 00 = ADC Fixed Voltage Reference Peripheral output is off 01 = ADC Fixed Voltage Reference Peripheral output is 1x (1.024V) 10 = ADC Fixed Voltage Reference Peripheral output is 2x (2.048V)⁽²⁾ 11 = ADC Fixed Voltage Reference Peripheral output is 4x (4.096V)⁽²⁾ 						
		ed Voltage Re	ference Peripl	heral output is) (PIC16F1825	4x (4.096V) ⁽²⁾		

REGISTER 14-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

2: Fixed Voltage Reference output cannot exceed VDD.

TABLE 14-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE FIXED VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR1	CDAFVR0	ADFVR1	ADFVR0	148

Legend: Shaded cells are unused by the Fixed Voltage Reference module.

15.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit's range of operating temperature falls between -40°C and +85°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately. Reference Application Note AN1333, *"Use and Calibration of the Internal Temperature Indicator"* (DS01333) for more details regarding the calibration process.

15.1 Circuit Operation

Figure 15-1 shows a simplified block diagram of the temperature circuit. The proportional voltage output is achieved by measuring the forward voltage drop across multiple silicon junctions.

Equation 15-1 describes the output characteristics of the temperature indicator.

EQUATION 15-1: VOUT RANGES

High Range: VOUT = VDD - 4VT

Low Range: VOUT = VDD - 2VT

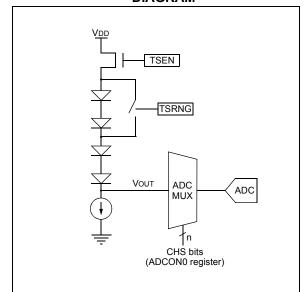
The temperature sense circuit is integrated with the Fixed Voltage Reference (FVR) module. See **Section 14.0 "Fixed Voltage Reference (FVR)"** for more information.

The circuit is enabled by setting the TSEN bit of the FVRCON register. When disabled, the circuit draws no current.

The circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range, but may be less consistent from part to part. This range requires a higher bias voltage to operate and thus, a higher VDD is needed.

The low range is selected by clearing the TSRNG bit of the FVRCON register. The low range generates a lower voltage drop and thus, a lower bias voltage is needed to operate the circuit. The low range is provided for low voltage operation.

FIGURE 15-1: TEMPERATURE CIRCUIT DIAGRAM



15.2 Minimum Operating VDD vs. Minimum Sensing Temperature

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 15-1 shows the recommended minimum VDD vs. range setting.

TABLE 15-1: RECOMMENDED VDD VS. RANGE

Min. VDD, TSRNG = 1	Min. VDD, TSRNG = 0
3.6V	1.8V

15.3 Temperature Output

The output of the circuit is measured using the internal analog to digital converter. Channel 29 is reserved for the temperature circuit output. Refer to Section 16.0 "Analog-to-Digital Converter (ADC) Module" for detailed information. NOTES:

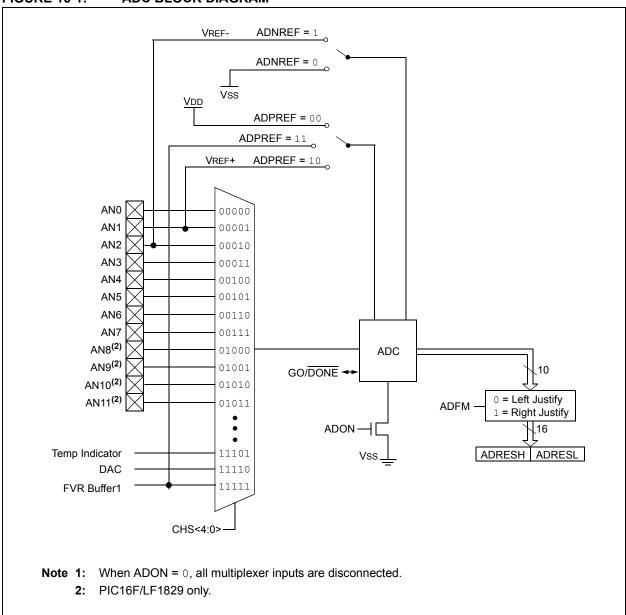
16.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 16-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

FIGURE 16-1: ADC BLOCK DIAGRAM

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.



16.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- · Port configuration
- · Channel selection
- · ADC voltage reference selection
- · ADC conversion clock source
- · Interrupt control
- · Result formatting

16.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to Section 12.0 "I/O Ports" for more information.

Note:	Analog voltages on any pin that is defined
	as a digital input may cause the input buf-
	fer to conduct excess current.

16.1.2 CHANNEL SELECTION

There are up to 15 channel selections available:

- AN<7:0> pins (PIC16F/LF1825 only)
- AN<11:0> pins (PIC16F/LF1829 only)
- Temperature Indicator
- · DAC Output
- · FVR (Fixed Voltage Reference) Output

Refer to Section 17.0 "Digital-to-Analog Converter (DAC) Module", Section 14.0 "Fixed Voltage Reference (FVR)" and Section 15.0 "Temperature Indicator Module" for more information on these channel selections.

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 16.2 "ADC Operation"** for more information.

16.1.3 ADC VOLTAGE REFERENCE

The ADPREF bits of the ADCON1 register provides control of the positive voltage reference. The positive voltage reference can be:

- VREF+ pin
- VDD
- FVR 2.048V
- FVR 4.096V (Not available on LF devices)

The ADNREF bits of the ADCON1 register provides control of the negative voltage reference. The negative voltage reference can be:

- VREF- pin
- Vss

See Section 14.0 "Fixed Voltage Reference (FVR)" for more details on the fixed voltage reference.

PIC16F/LF1825/1829

16.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11.5 TAD periods as shown in Figure 16-2.

For correct conversion, the appropriate TAD specification must be met. Refer to the A/D conversion requirements in **Section 30.0 "Electrical Specifications"** for more information. Table 16-1 gives examples of appropriate ADC clock selections.

Note:									
	system clock frequency will change the								
	ADC clock frequency, which may								
	adversely affect the ADC result.								

TABLE 16-1: ADC CLOCK PERIOD (TAD) Vs. DEVICE OPERATING FREQUENCIES

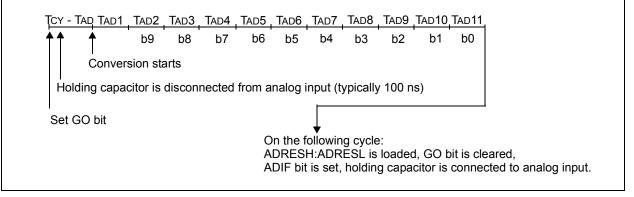
ADC Clock Period (TAD)		Device Frequency (Fosc)						
ADC Clock Source	ADCS<2:0>	32 MHz	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz	
Fosc/2	000	62.5ns ⁽²⁾	100 ns ⁽²⁾	125 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	2.0 μs	
Fosc/4	100	125 ns ⁽²⁾	200 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	1.0 μs	4.0 μs	
Fosc/8	001	0.5 μs ⁽²⁾	400 ns ⁽²⁾	0.5 μs ⁽²⁾	1.0 μs	2.0 μs	8.0 μs ⁽³⁾	
Fosc/16	101	800 ns	800 ns	1.0 μs	2.0 μs	4.0 μs	16.0 μs ⁽³⁾	
Fosc/32	010	1.0 μs	1.6 μs	2.0 μs	4.0 μs	8.0 μs ⁽³⁾	32.0 μs ⁽³⁾	
Fosc/64	110	2.0 μs	3.2 μs	4.0 μs	8.0 μs ⁽³⁾	16.0 μs ⁽³⁾	64.0 μs ⁽³⁾	
FRC	x11	1.0-6.0 μs ^(1,4)						

Legend: Shaded cells are outside of recommended range.

- Note 1: The FRC source has a typical TAD time of 1.6 μ s for VDD.
 - **2:** These values violate the minimum required TAD time.
 - 3: For faster conversion times, the selection of another clock source is recommended.

4: The ADC clock period (TAD) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock FOSC. However, the FRC clock source must be used when conversions are to be performed with the device in Sleep mode.

FIGURE 16-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES



16.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note 1:	The ADIF bit is set at the completion of
	every conversion, regardless of whether
	or not the ADC interrupt is enabled.

2: The ADC operates during Sleep only when the FRC oscillator is selected.

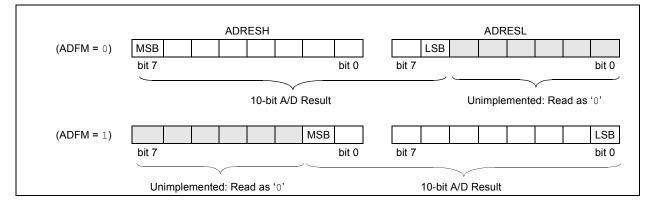
This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

16.1.6 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON1 register controls the output format.

Figure 16-3 shows the two output formats.

FIGURE 16-3: 10-BIT A/D CONVERSION RESULT FORMAT



16.2 ADC Operation

16.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/ DONE bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note:	The GO/DONE bit should not be set in the
	same instruction that turns on the ADC.
	Refer to Section 16.2.6 "A/D Conver-
	sion Procedure".

16.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONE bit
- · Set the ADIF Interrupt Flag bit
- Update the ADRESH and ADRESL registers with new conversion result

16.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRESH and ADRESL registers will be updated with the partially complete Analog-to-Digital conversion sample. Incomplete bits will match the last bit converted.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

16.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

16.2.5 SPECIAL EVENT TRIGGER

The Special Event Trigger of the CCPx/ECCPX module allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/DONE bit is set by hardware and the Timer1 counter resets to zero.

TABLE 16-2: SPECIAL EVENT TRIGGER

Device	CCPx/ECCPx			
PIC16F/LF1825/1829	CCP4			

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

Refer to Section 24.0 "Capture/Compare/PWM Modules" for more information.

16.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

- 1. Configure Port:
 - Disable pin output driver (Refer to the TRIS register)
 - Configure pin as analog (Refer to the ANSEL register)
- 2. Configure the ADC module:
 - Select ADC conversion clock
 - Configure voltage reference
 - Select ADC input channel
 - Turn on ADC module
- 3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - Enable ADC interrupt
 - Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
- 4. Wait the required acquisition time⁽²⁾.
- 5. Start conversion by setting the GO/DONE bit.
- 6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt (interrupts enabled)
- 7. Read ADC Result.
- 8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: Refer to Section 16.3 "A/D Acquisition Requirements".

EXAMPLE 16-1: A/D CONVERSION

;This code block configures the ADC ;for polling, Vdd and Vss references, Frc ;clock and ANO input. ;

;Conversion start & polling for completion ; are included.

;		
BANKSEL	ADCON1	;
MOVLW	B'11110000'	;Right justify, Frc
		;clock
MOVWF	ADCON1	;Vdd and Vss Vref
BANKSEL	TRISA	;
BSF	TRISA,0	;Set RAO to input
BANKSEL	ANSEL	;
BSF	ANSEL,0	;Set RA0 to analog
BANKSEL	ADCON0	;
MOVLW	B'0000001'	;Select channel ANO
MOVWF	ADCON0	;Turn ADC On
CALL	SampleTime	;Acquisiton delay
BSF	ADCON0, ADGO	;Start conversion
BTFSC	ADCON0, ADGO	;Is conversion done?
GOTO	\$-1	;No, test again
BANKSEL	ADRESH	;
MOVF	ADRESH,W	;Read upper 2 bits
MOVWF	RESULTHI	;store in GPR space
BANKSEL	ADRESL	;
MOVF	ADRESL,W	;Read lower 8 bits
MOVWF	RESULTLO	;Store in GPR space

16.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

REGISTER 16-1: ADCON0: A/D CONTROL REGISTER 0

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—			CHS<4:0>			GO/DONE	ADON
bit 7							bit 0

Legend:							
R = Readable bit		W = Writable bit	U = Unimplemented bit, read as '0'				
u = Bit is unchanged		x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit i	s set	'0' = Bit is cleared					
bit 7	Unimpler	mented: Read as '0'					
bit 6-2	CHS<4:0	>: Analog Channel Select bits	3				
	00000 =	AN0					
	00001 =	AN1					
	00010 =						
	00011 =	-					
	00100 =						
	00101 = 00110 =						
	00110 =						
	01000 =						
	01001 =						
	01010 =	AN10 ⁽¹⁾					
	01011 =						
	01100 =	Reserved. No channel conne	ected.				
	•						
	•						
	11100 =	Reserved. No channel conne	octed				
		Temperature Indicator ⁽⁴⁾					
		DAC output ⁽²⁾					
	111 <u>11 = </u>	FVR (Fixed Voltage Referenc	e) Buffer 1 Output ⁽³⁾				
bit 1	GO/DONE: A/D Conversion Status bit						
	1 = A/D c	onversion cycle in progress.	Setting this bit starts an A/D conversion cycle.				
			hardware when the A/D conversion has completed.				
	0 = A/D c	onversion completed/not in p	rogress				
bit 0	ADON: A	DC Enable bit					
	-	is enabled					
	0 = ADC	is disabled and consumes no	operating current				
Note 1:	PIC16F/LF182	29 only.					
2:	See Section 1	7.0 "Digital-to-Analog Conv	verter (DAC) Module" for more information.				
3:	See Section 1	4.0 "Fixed Voltage Referen	ce (FVR)" for more information.				
4:	See Section 1	5.0 "Temperature Indicator	Module" for more information.				
		•					

PIC16F/LF1825/1829

R/W-0/	0 R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM		ADCS<2:0>			ADNREF	ADPRE	F<1:0>
bit 7	·						bit 0
1							
Legend:			L:1			(O'	
R = Reada		W = Writable		•	nented bit, read		athar Daaata
	inchanged	x = Bit is unkr		-n/n = value a	at POR and BO	R/value at all	other Resets
'1' = Bit is	set	'0' = Bit is clea	ared				
bit 7	1 = Right ji loaded	stified. Six Least	Significant bi				
bit 6-4	000 = Fos 001 = Fos 010 = Fos 011 = FRC 100 = Fos 101 = Fos 110 = Fos	c/8 c/32 (clock supplied f c/4 c/16	rom a dedicat	ed RC oscillato			
bit 3	Unimplem	ented: Read as ') '				
bit 2	0 = VREF-	A/D Negative Voli - is connected to - is connected to	Vss	C C	ı bit		
bit 1-0	ADPREF<1 00 = VREF- 01 = Resen 10 = VREF-	1:0>: A/D Positive + is connected to	e Voltage Refe VDD external VREF	erence Configui -+ pin ⁽¹⁾		dule ⁽¹⁾	
Note 1:	•	the FVR or the V e specification ex	•		•		

REGISTER 16-3: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
			ADRE	S<9:2>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimpler	mented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkn	iown	-n/n = Value a	at POR and BC	R/Value at all	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				

bit 7-0 ADRES<9:2>: ADC Result Register bits Upper 8 bits of 10-bit conversion result

REGISTER 16-4: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<1:0>		—	—	—	—	_	_
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 ADRES<1:0>: ADC Result Register bits Lower 2 bits of 10-bit conversion result

bit 5-0 **Reserved**: Do not use.

REGISTER 16-5: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
-	—	—	—	_	_	ADRE	S<9:8>
bit 7	•			•			bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				

 bit 7-2
 Reserved: Do not use.

 bit 1-0
 ADRES<9:8>: ADC Result Register bits Upper 2 bits of 10-bit conversion result

REGISTER 16-6: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

| R/W-x/u |
|---------|---------|---------|---------|---------|---------|---------|---------|
| | | | ADRES | 6<7:0> | | | |
| bit 7 | | | | | | | bit 0 |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 ADRES<7:0>: ADC Result Register bits Lower 8 bits of 10-bit conversion result

16.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 16-4. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), refer to Figure 16-4. The maximum recommended impedance for analog sources is 10 k Ω . As the

source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 16-1 may be used. This equation assumes that 1/2 LSb error is used (1,024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 16-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature =
$$50^{\circ}C$$
 and external impedance of $10k\Omega 5.0V VDD$
 $TACQ = Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient$
 $= TAMP + TC + TCOFF$
 $= 2\mu s + TC + [(Temperature - 25^{\circ}C)(0.05\mu s/^{\circ}C)]$

The value for TC can be approximated with the following equations:

$$V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = V_{CHOLD} ; [1] V_{CHOLD} charged to within 1/2 lsb$$

$$V_{APPLIED}\left(1 - e^{\frac{-Tc}{RC}}\right) = V_{CHOLD} ; [2] V_{CHOLD} charge response to V_{APPLIED} (1 - \frac{1}{(2^{n+1}) - 1}) ; combining [1] and [2]$$

Note: Where n = number *of bits of the ADC.*

Solving for TC:

$$TC = -C_{HOLD}(RIC + RSS + RS) \ln(1/511)$$

= $-10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.001957)$
= $1.12\mu s$

Therefore:

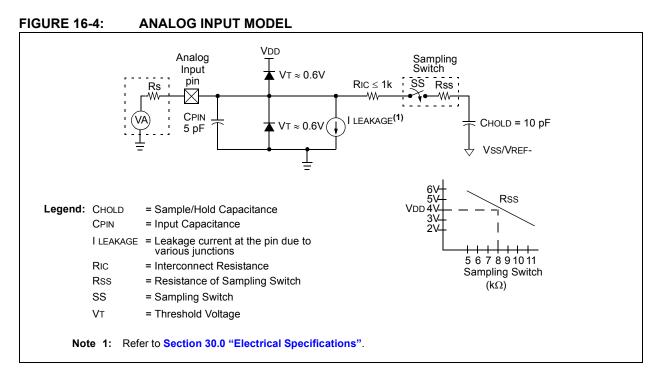
$$TACQ = 2\mu s + 1.12\mu s + [(50^{\circ}C - 25^{\circ}C)(0.05\mu s/^{\circ}C)]$$

= 4.42\mu s

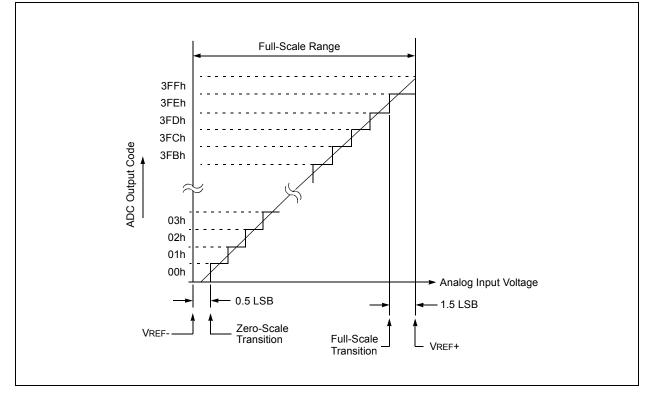
Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

- 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
- **3:** The maximum recommended impedance for analog sources is $10 \text{ k}\Omega$. This is required to meet the pin leakage specification.

PIC16F/LF1825/1829







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DS41440A-page 163

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	_	CHS4	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	158
ADCON1	ADFM	ADCS2	ADCS1	ADCS0	—	ADNREF	ADPREF1	ADPREF0	159
ADRESH	A/D Result Re	egister High							160, 161
ADRESL	A/D Result Re	egister Low							160, 161
ANSELA	—	_	_	ANSA4	_	ANSA2	ANSA1	ANSA0	130
ANSELB ⁽¹⁾	ANSB7	ANSB6	ANSB5	ANSB4	—	—	—	—	136
ANSELC	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	_	_	ANSC3	ANSC2	ANSC1	ANSC0	141
CCP4CON	P4M1	P4M0	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	240
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	_	_	_	—	136
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
TRISA	—	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	—	_	—	—	135
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR1	CDAFVR0	ADFVR1	ADFVR0	148
DACCON0	DACEN	DACLPS	DACOE	—	DACPSS1	DACPSS0	—	DACNSS	168
DACCON1	—	—	—	DACR4	DACR3	DACR2	DACR1	DACR0	168

TABLE 16-3: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for ADC module. PIC16F/LF1829 only. Legend:

Note 1:

17.0 DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DACOUT pin

The Digital-to-Analog Converter (DAC) can be enabled by setting the DACEN bit of the DACCON0 register.

17.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DACR<4:0> bits of the DACCON1 register.

The DAC output voltage is determined by the following equations:

EQUATION 17-1: DAC OUTPUT VOLTAGE

$$Vout = \left((Vsource+ - Vsource-) \times \frac{DACR < 4:0>}{2^5} \right) + Vsrc-$$
Note: Vsource+ can equal FVR Buffer 2, VDD or VREF+. Vsource- can equal Vss or VREF-.

17.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in **Section 30.0** "**Electrical Specifications**".

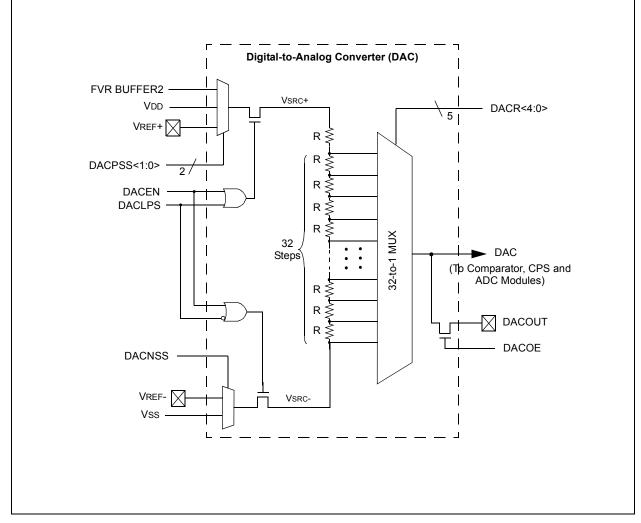
17.3 DAC Voltage Reference Output

The DAC can be output to the DACOUT pin by setting the DACOE bit of the DACCON0 register to '1'. Selecting the DAC reference voltage for output on the DACOUT pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DACOUT pin when it has been configured for DAC reference voltage output will always return a '0'.

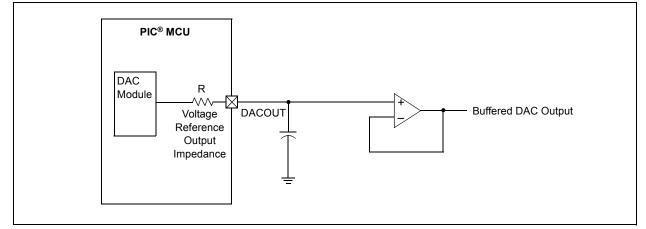
Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to DACOUT. Figure 17.5 shows an example buffering technique.

PIC16F/LF1825/1829

FIGURE 17-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM







17.4 Low-Power Voltage State

In order for the DAC module to consume the least amount of power, one of the two voltage reference input sources to the resistor ladder must be disconnected. Either the positive voltage source, (VSRC+), or the negative voltage source, (VSRC-) can be disabled.

The negative voltage source is disabled by setting the DACLPS bit in the DACCON0 register. Clearing the DACLPS bit in the DACCON0 register disables the positive voltage source.

17.4.1 OUTPUT CLAMPED TO POSITIVE VOLTAGE SOURCE

The DAC output voltage can be set to VSRC+ with the least amount of power consumption by performing the following:

- · Clearing the DACEN bit in the DACCON0 register.
- Setting the DACLPS bit in the DACCON0 register.
- Configuring the DACPSS bits to the proper positive source.
- Configuring the DACR<4:0> bits to '11111' in the DACCON1 register.

This is also the method used to output the voltage level from the FVR to an output pin. See **Section 17.5 "Operation During Sleep"** for more information.

Reference Figure 17-3 for output clamping examples.

17.4.2 OUTPUT CLAMPED TO NEGATIVE VOLTAGE SOURCE

The DAC output voltage can be set to VsRc- with the least amount of power consumption by performing the following:

- · Clearing the DACEN bit in the DACCON0 register.
- Clearing the DACLPS bit in the DACCON0 register.
- Configuring the DACNSS bits to the proper negative source.

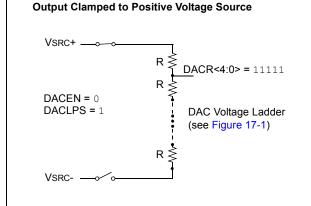
Output Clamped to Negative Voltage Source

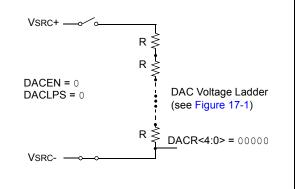
• Configuring the DACR<4:0> bits to '00000' in the DACCON1 register.

This allows the comparator to detect a zero-crossing while not consuming additional current through the DAC module.

Reference Figure 17-3 for output clamping examples.

FIGURE 17-3: OUTPUT VOLTAGE CLAMPING EXAMPLES





17.5 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the DACCON0 register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

17.6 Effects of a Reset

A device Reset affects the following:

- DAC is disabled.
- DAC output voltage is removed from the DACOUT pin.
- The DACR<4:0> range select bits are cleared.
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R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
DACEN	DACLPS	DACOE	—	DACPS	SS<1:0>	—	DACNSS
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	as '0'	
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	DACEN: DAG						
	1 = DAC is enabled 0 = DAC is disabled						
bit 6		AC Low-Power	Voltago Stato	Select hit			
bit 0		sitive reference	-				
		gative reference					
bit 5	DACOE: DAG	C Voltage Outpu	ut Enable bit				
		tage level is als					
		tage level is dis		om the DACOU	T pin		
bit 4	Unimplemen	ited: Read as '	2'				
bit 3-2		0>: DAC Positiv	e Source Sel	ect bits			
	00 = VDD 01 = VREF+						
	10 = FVR Buffer2 output						
		ed, do not use					
bit 1	Unimplemen	ted: Read as '	o'				
bit 0	DACNSS: DA	AC Negative So	urce Select b	its			
	1 = VREF-						
	0 = Vss						

REGISTER 17-1: DACCON0: VOLTAGE REFERENCE CONTROL REGISTER 0

REGISTER 17-2: DACCON1: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—			DACR<4:0>		
bit 7							bit 0

Legend:						
R = Readable bit		W = Writable bit	U = Unimplemented bit, read as '0'			
u = Bit is u	nchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets			
'1' = Bit is	set	'0' = Bit is cleared				
bit 7-5	bit 7-5 Unimplemented: Read as '0'					
bit 4-0	DACR<4:0>: DAC Voltage Output Select bits					
$VOUT = ((VSRC+) - (VSRC-))^*(DACR < 4:0 > /(2^5)) + VSRC-$						

Note 1: The output select bits are always right justified to ensure that any number of bits can be used without affecting the register layout

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR1	CDAFVR0	ADFVR1	ADFVR0	148
DACCON0	DACEN	DACLPS	DACOE	-	DACPSS1	DACPSS0	_	DACNSS	168
DACCON1	_			DACR4	DACR3	DACR2	DACR1	DACR0	168

TABLE 17-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE DAC MODULE

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the DAC module.

NOTES:

18.0 SR LATCH

The module consists of a single SR Latch with multiple Set and Reset inputs as well as separate latch outputs. The SR Latch module includes the following features:

- · Programmable input selection
- SR Latch output is available externally
- Separate Q and \overline{Q} outputs
- · Firmware Set and Reset

The SR Latch can be used in a variety of analog applications, including oscillator circuits, one-shot circuit, hysteretic controllers, and analog timing applications.

18.1 Latch Operation

The latch is a Set-Reset Latch that does not depend on a clock source. Each of the Set and Reset inputs are active-high. The latch can be Set or Reset by:

- Software control (SRPS and SRPR bits)
- Comparator C1 output (SYNCC1OUT)
- Comparator C2 output (SYNCC2OUT) (PIC16F/LF1829 only)
- SRI pin
- Programmable clock (SRCLK)

The SRPS and the SRPR bits of the SRCON0 register may be used to Set or Reset the SR Latch, respectively. The latch is Reset-dominant. Therefore, if both Set and Reset inputs are high, the latch will go to the Reset state. Both the SRPS and SRPR bits are self resetting which means that a single write to either of the bits is all that is necessary to complete a latch Set or Reset operation.

The output from Comparator C1 or C2 can be used as the Set or Reset inputs of the SR Latch. The output of either Comparator can be synchronized to the Timer1 clock source. See Section 19.0 "Comparator Module" and Section 21.0 "Timer1 Module with Gate Control" for more information.

An external source on the SRI pin can be used as the Set or Reset inputs of the SR Latch.

An internal clock source is available that can periodically Set or Reset the SR Latch. The SRCLK<2:0> bits in the SRCON0 register are used to select the clock source period. The SRSCKE and SRRCKE bits of the SRCON1 register enable the clock source to Set or Reset the SR Latch, respectively.

Note: Enabling both the Set and Reset inputs from any one source at the same time may result in indeterminate operation, as the Reset dominance cannot be assured.

18.2 Latch Output

The SRQEN and SRNQEN bits of the SRCON0 register control the Q and \overline{Q} latch outputs. Both of the SR Latch outputs may be directly output to an I/O pin at the same time.

The applicable TRIS bit of the corresponding port must be cleared to enable the port pin output driver.

18.3 Effects of a Reset

Upon any device Reset, the SR Latch output is not initialized to a known state. The user's firmware is responsible for initializing the latch output before enabling the output pins.

PIC16F/LF1825/1829

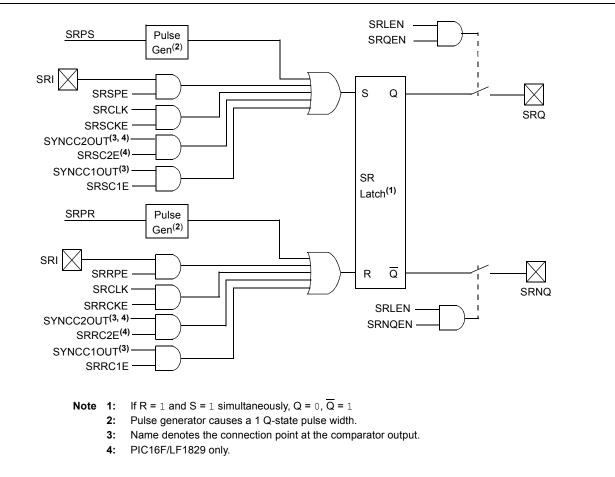


FIGURE 18-1: SR LATCH SIMPLIFIED BLOCK DIAGRAM

SRCLK	Divider	Fosc = 32 MHz	Fosc = 20 MHz	Fosc = 16 MHz	Fosc = 4 MHz	Fosc = 1 MHz
111	512	62.5 kHz	39.0 kHz	31.3 kHz	7.81 kHz	1.95 kHz
110	256	125 kHz	78.1 kHz	62.5 kHz	15.6 kHz	3.90 kHz
101	128	250 kHz	156 kHz	125 kHz	31.25 kHz	7.81 kHz
100	64	500 kHz	313 kHz	250 kHz	62.5 kHz	15.6 kHz
011	32	1 MHz	625 kHz	500 kHz	125 kHz	31.3 kHz
010	16	2 MHz	1.25 MHz	1 MHz	250 kHz	62.5 kHz
001	8	4 MHz	2.5 MHz	2 MHz	500 kHz	125 kHz
000	4	8 MHz	5 MHz	4 MHz	1 MHz	250 kHz

TABLE 18-1: SRCLK FREQUENCY TABLE

REGISTER 18-1: SRCON0: SR LATCH CONTROL 0 REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/S-0/0	R/S-0/0
SRLEN	SRCLK2	SRCLK1	SRCLK0	SRQEN	SRNQEN	SRPS	SRPR
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	S = Bit is set only

bit 7	SRLEN: SR Latch Enable bit 1 = SR Latch is enabled 0 = SR Latch is disabled			
bit 6-4	SRCLK<2:0>: SR Latch Clock Divider bits 000 = Generates a 1 Fosc wide pulse every 4th Fosc cycle clock 001 = Generates a 1 Fosc wide pulse every 8th Fosc cycle clock 010 = Generates a 1 Fosc wide pulse every 16th Fosc cycle clock 011 = Generates a 1 Fosc wide pulse every 32nd Fosc cycle clock 100 = Generates a 1 Fosc wide pulse every 64th Fosc cycle clock 101 = Generates a 1 Fosc wide pulse every 128th Fosc cycle clock 110 = Generates a 1 Fosc wide pulse every 256th Fosc cycle clock 111 = Generates a 1 Fosc wide pulse every 512th Fosc cycle clock			
bit 3	<pre>SRQEN: SR Latch Q Output Enable bit If SRLEN = 1: 1 = Q is present on the SRQ pin 0 = External Q output is disabled If SRLEN = 0: SR Latch is disabled</pre>			
bit 2	SRNQEN: SR Latch Q Output Enable bit If SRLEN = 1: 1 = Q is present on the SRnQ pin 0 = External Q output is disabled If SRLEN = 0: SR Latch is disabled			
bit 1	 SRPS: Pulse Set Input of the SR Latch bit⁽¹⁾ 1 = Pulse set input for 1 Q-clock period 0 = No effect on set input. 			
bit 0	 SRPR: Pulse Reset Input of the SR Latch bit⁽¹⁾ 1 = Pulse Reset input for 1 Q-clock period 0 = No effect on Reset input. 			
	and a shure we also have to (2)			

Note 1: Set only, always reads back '0'.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
SRSPE	SRSCKE	SRSC2E ⁽¹⁾	SRSC1E	SRRPE	SRRCKE	SRRC2E ⁽¹⁾	SRRC1E	
bit 7	SKOCKE	SK302E	SKOUTE	SKKFE	SKRCRE	SKRC2E.	bit 0	
DIL 7							DILU	
Legend:								
R = Readable	, hit	\\/ = \\/ritabla	t	II – Unimplor	monted hit read			
		W = Writable I		U = Unimplemented bit, read as '0'				
u = Bit is unch	•	x = Bit is unknown -n/n = Value at POR and BOR/Value at all other					other Resets	
'1' = Bit is set		'0' = Bit is clea	ared					
bit 7		Latch Periphera						
		h is set when the has no effect on			2			
bit 6	•	R Latch Set Clo	•	OI THE SK LAC	1			
DILO								
	 1 = Set input of SR Latch is pulsed with SRCLK 0 = SRCLK has no effect on the set input of the SR Latch 							
bit 5		R Latch C2 Set I						
		h is set when th		ator output is hi	iah			
		parator output h				h		
bit 4	SRSC1E: SF	R Latch C1 Set I	Enable bit					
		h is set when th						
	0 = C1 Comparator output has no effect on the set input of the SR Latch							
bit 3	·							
1 = SR Latch is reset when the SRI pin is high								
0 = SRI pin has no effect on the Reset input of the SR Latch								
DIT 2	bit 2 SRRCKE: SR Latch Reset Clock Enable bit							
	 1 = Reset input of SR Latch is pulsed with SRCLK 0 = SRCLK has no effect on the Reset input of the SR Latch 							
bit 1 SRRC2E: SR Latch C2 Reset Enable bit ⁽¹⁾								
1 = SR Latch is reset when the C2 Comparator output is high								
		parator output h				atch		
bit 0	SRRC1E: SF	R Latch C1 Rese	et Enable bit					
	1 = SR Latch is reset when the C1 Comparator output is high							
	0 = C1 Comparator output has no effect on the Reset input of the SR Latch							
Note 1: PIG	C16F/LF1829 o	only.						

REGISTER 18-2: SRCON1: SR LATCH CONTROL 1 REGISTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—		—	ANSA4		ANSA2	ANSA1	ANSA0	130
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
SRCON0	SRLEN	SRCLK2	SRCLK1	SRCLK0	SRQEN	SRNQEN	SRPS	SRPR	173
SRCON1	SRSPE	SRSCKE	SRSC2E ⁽¹⁾	SRSC1E	SRRPE	SRRCKE	SRRC2E ⁽¹⁾	SRRC1E	174
TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140

 TABLE 18-2:
 SUMMARY OF REGISTERS ASSOCIATED WITH SR LATCH MODULE

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the SR Latch module.

Note 1: PIC16F/LF1829 only.

NOTES:

19.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- · Independent comparator control
- Programmable input selection
- · Comparator output is available internally/externally
- · Programmable output polarity
- Interrupt-on-change
- · Wake-up from Sleep
- Programmable Speed/Power optimization
- PWM shutdown
- · Programmable and fixed voltage reference

19.1 Comparator Overview

A single comparator is shown in Figure 19-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the

comparator is a digital low level. When the analog voltage at V_{IN+} is greater than the analog voltage at V_{IN-} , the output of the comparator is a digital high level.

FIGURE 19-1: SINGLE COMPARATOR

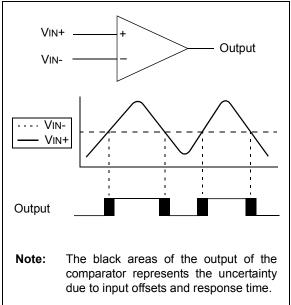
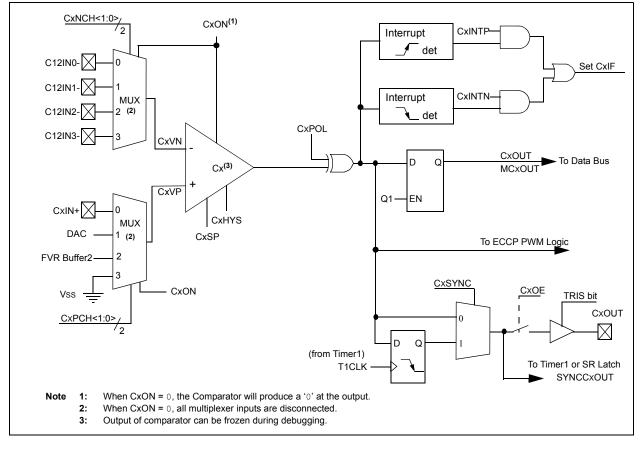


FIGURE 19-2: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM



19.2 Comparator Control

Each comparator has 2 control registers: CMxCON0 and CMxCON1.

The CMxCON0 registers (see Register 19-1) contain Control and Status bits for the following:

- Enable
- · Output selection
- Output polarity
- · Speed/Power selection
- · Hysteresis enable
- · Output synchronization

The CMxCON1 registers (see Register 19-2) contain Control bits for the following:

- · Interrupt enable
- · Interrupt edge polarity
- · Positive input channel selection
- Negative input channel selection

19.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

19.2.2 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register. In order to make the output available for an external connection, the following conditions must be true:

- · CxOE bit of the CMxCON0 register must be set
- · Corresponding TRIS bit must be cleared
- · CxON bit of the CMxCON0 register must be set

Note 1:	The CxOE bit of the CMxCON0 register
	overrides the PORT data latch. Setting
	the CxON bit of the CMxCON0 register
	has no impact on the port override.

2: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

19.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 19-1 shows the output state versus input conditions, including polarity control.

TABLE 19-1:COMPARATOR OUTPUT
STATE VS. INPUT
CONDITIONS

Input Condition	CxPOL	CxOUT
CxVN > CxVP	0	0
CxVN < CxVP	0	1
CxVN > CxVP	1	0
CxVN < CxVP	1	1

19.2.4 COMPARATOR SPEED/POWER SELECTION

The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is '1' which selects the normal speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to '0'.

19.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit of the CMxCON0 register.

See **Section 30.0 "Electrical Specifications**" for more information.

19.4 Timer1 Gate Operation

The output resulting from a comparator operation can be used as a source for gate control of Timer1. See **Section 21.6 "Timer1 Gate"** for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to Timer1. This ensures that Timer1 does not increment while a change in the comparator is occurring.

19.4.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from either comparator, C1 or C2, can be synchronized with Timer1 by setting the CxSYNC bit of the CMxCON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 19-2) and the Timer1 Block Diagram (Figure 21-1) for more information.

19.5 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator, a rising edge detector and a Falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (CxINTP and/or CxINTN bits of the CMxCON1 register), the Corresponding Interrupt Flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, you must set the following bits:

- CxON, CxPOL and CxSP bits of the CMxCON0 register
- CxIE bit of the PIE2 register
- CxINTP bit of the CMxCON1 register (for a rising edge detection)
- CxINTN bit of the CMxCON1 register (for a falling edge detection)
- · PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

Note: Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the CxPOL bit of the CMxCON0 register, or by switching the comparator on or off with the CxON bit of the CMxCON0 register.

19.6 Comparator Positive Input Selection

Configuring the CxPCH<1:0> bits of the CMxCON1 register directs an internal voltage reference or an analog pin to the non-inverting input of the comparator:

- CxIN+ analog pin
- DAC
- FVR (Fixed Voltage Reference)
- · Vss (Ground)

See **Section 14.0 "Fixed Voltage Reference (FVR)"** for more information on the Fixed Voltage Reference module.

See Section 17.0 "Digital-to-Analog Converter (DAC) Module" for more information on the DAC input signal.

Any time the comparator is disabled (CxON = 0), all comparator inputs are disabled.

19.7 Comparator Negative Input Selection

The CxNCH<1:0> bits of the CMxCON0 register direct one of four analog pins to the comparator inverting input.

Note:	To use CxIN+ and CxINx- pins as analog
	input, the appropriate bits must be set in
	the ANSEL register and the correspond-
	ing TRIS bits must also be set to disable
	the output drivers.

19.8 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in Section 30.0 "Electrical Specifications" for more details.

19.9 Interaction with ECCP Logic

The C1 and C2 comparators can be used as general purpose comparators. Their outputs can be brought out to the C1OUT and C2OUT pins. When the ECCP auto-shutdown is active it can use one or both comparator signals. If auto-restart is also enabled, the comparators can be configured as a closed loop analog feedback to the ECCP, thereby, creating an analog controlled PWM.

Note: When the comparator module is first initialized the output state is unknown. Upon initialization, the user should verify the output state of the comparator prior to relying on the result, primarily when using the result in connection with other peripheral features, such as the ECCP Auto-Shutdown mode.

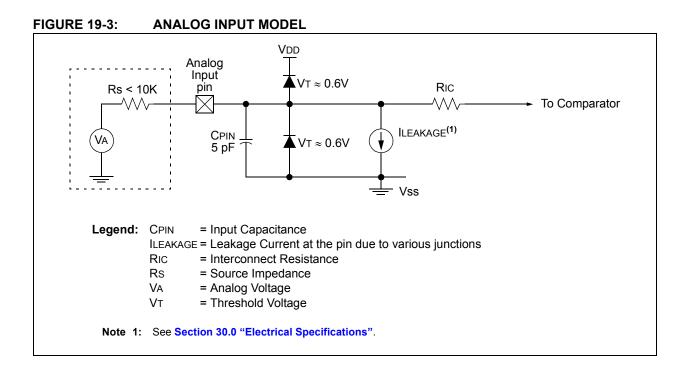
19.10 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 19-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of $10 \text{ k}\Omega$ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

> Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.



CxON bit 7 Legend: R = Readable u = Bit is unch '1' = Bit is set bit 7 bit 6	tranged x = '0' : CxON: Comparate 1 = Comparator is 0 = Comparator is CxOUT: Comparator is If CxPOL = 1 (investigation)	enabled a disabled	nown ared	-n/n = Value	CxSP emented bit, read at POR and BC		CxSYNC bit 0			
Legend: R = Readable u = Bit is unch '1' = Bit is set bit 7	tranged x = '0' : CxON: Comparate 1 = Comparator is 0 = Comparator is CxOUT: Comparator is If CxPOL = 1 (investigation)	Bit is unkr = Bit is clea or Enable l = enabled a = disabled	nown ared	-n/n = Value	at POR and BC					
R = Readable u = Bit is unch '1' = Bit is set bit 7	tranged x = '0' : CxON: Comparate 1 = Comparator is 0 = Comparator is CxOUT: Comparator is If CxPOL = 1 (investigation)	Bit is unkr = Bit is clea or Enable l = enabled a = disabled	nown ared	-n/n = Value	at POR and BC		other Resets			
R = Readable u = Bit is unch '1' = Bit is set bit 7	tranged x = '0' : CxON: Comparate 1 = Comparator is 0 = Comparator is CxOUT: Comparator is If CxPOL = 1 (investigation)	Bit is unkr = Bit is clea or Enable l = enabled a = disabled	nown ared	-n/n = Value	at POR and BC		other Resets			
u = Bit is unch '1' = Bit is set bit 7	tranged x = '0' : CxON: Comparate 1 = Comparator is 0 = Comparator is CxOUT: Comparator is If CxPOL = 1 (investigation)	Bit is unkr = Bit is clea or Enable l = enabled a = disabled	nown ared	-n/n = Value	at POR and BC		other Resets			
ʻ1' = Bit is set bit 7	^{(0'} : CxON: Comparator 1 = Comparator is 0 = Comparator is CxOUT: Compara If CxPOL = 1 (investigation)	= Bit is clea or Enable I enabled a disabled	ared							
bit 7	CxON: Comparato 1 = Comparator is 0 = Comparator is CxOUT: Compara If CxPOL = 1 (inve	or Enable I enabled a disabled	bit	no active pov						
	1 = Comparator is 0 = Comparator is CxOUT: Compara <u>If CxPOL = 1 (inve</u>	enabled a disabled		no active pov	vor					
bit 6	0 = Comparator is CxOUT: Compara If CxPOL = 1 (inve	disabled	and consumes	no active pov	vor					
bit 6	CxOUT: Compara				vei					
bit 6	If CxPOL = 1 (inve	tor Output								
			<u>ity):</u>							
	1 = CxVP < CxVN 0 = CxVP > CxVN									
	1100000000000000000000000000000000000		<u>oolarity):</u>							
	1 = CxVP > CxVI									
	0 = CxVP < CxVI	-								
bit 5	CxOE: Comparate	•								
		is present on the CxOUT pin. Requires that the associated TRIS bit be cleared to actually pin. Not affected by CxON.								
	0 = CxOUT is integrated by the pint.		ed by CAON.							
bit 4	CxPOL: Compara	tor Output	Polarity Selec	ct bit						
	1 = Comparator o	ator output is inverted								
	0 = Comparator o	utput is no	t inverted							
bit 3	Unimplemented:	Read as '	0'							
bit 2	CxSP: Comparate	•								
		 = Comparator operates in normal power, higher speed mode = Comparator operates in low-power, low-speed mode 								
1. 11. A	•		•	•	2					
bit 1		kHYS: Comparator Hysteresis Enable bit Comparator hysteresis enabled								
	0 = Comparator h	•								
bit 0	CxSYNC: Compa	•		is Mode bit						
	1 = Comparator of	•	•		ronous to chance	ges on Timer1	clock source			
	Output updat	ed on the f	falling edge of	Timer1 clock	source.	,				
	0 = Comparator of	output to Ti	imer1 and I/O	pin is asynchr	ronous.					

REGISTER 19-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	
CxINTP	CxINTN CxPCH<1:0>			_	— CxNCH<1:0			
bit 7					•		bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'		
u = Bit is unch	nanged	x = Bit is unkr	iown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets	
'1' = Bit is set		'0' = Bit is clea	ared					
bit 7		nparator Interru	1	0 0				
					ing edge of the			
					of the CxOUT b	DIT		
bit 6		nparator Interru		•••				
				0 0	ping edge of the of the CxOUT			
bit 5-4		Comparator F	0	0 0 0		5 M		
		onnects to CxIN	•		510			
		onnects to DAC		rence				
		onnects to FVR	Voltage Refe	rence				
	$\frac{\text{For C1:}}{11 - CV/D}$	opposto to C12						
	For C2:	onnects to C12	int pin					
		connects to Vss						
bit 3-2	Unimplemen	ted: Read as '	o'					
bit 1-0	CxNCH<1:0>	: Comparator N	Vegative Input	Channel Sele	ct bits			
	00 = CxVN c	onnects to C12	IN0- pin					
		onnects to C12	•					
		onnects to C12						
	$\perp \perp = CXVNC$	onnects to C12	ing- biu					

REGISTER 19-2: CMxCON1: COMPARATOR Cx CONTROL REGISTER 1

REGISTER 19-3: CMOUT: COMPARATOR OUTPUT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R-0/0	R-0/0	
—	_	_	—	_	_	MC2OUT	MC1OUT	
bit 7 bit C								

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2	Unimplemented: Read as '0'

- bit 1 MC2OUT: Mirror Copy of C2OUT bit
- bit 0 MC10UT: Mirror Copy of C10UT bit

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Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CM1CON0	C10N	C10UT	C10E	C1POL	—	C1SP	C1HYS	C1SYNC	182
CM1CON1	C1NTP	C1INTN	C1PCH1	C1PCH0	_	_	C1NCH1	C1NCH0	183
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2SP	C2HYS	C2SYNC	182
CM2CON1	C2NTP	C2INTN	C2PCH1	C2PCH0	—	—	C2NCH1	C2NCH0	183
CMOUT	_	_	_	_	_	_	MC2OUT	MC10UT	183
DACCON0	DACEN	DACLPS	DACOE	_	DACPSS1	DACPSS0	_	DACNSS	168
DACCON1	—	—	_	DACR4	DACR3	DACR2	DACR1	DACR0	168
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR1	CDAFVR0	ADFVR1	ADFVR0	148
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	_	CCP2IE	95
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	99
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	140
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	140
TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140

TABLE 19-2: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.

Note 1: PIC16F/LF1829 only.

20.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (independent of Watchdog Timer)
- · Programmable internal or external clock source
- · Programmable external clock edge selection
- Interrupt on overflow
- TMR0 can be used to gate Timer1

Figure 20-1 is a block diagram of the Timer0 module.

20.1 Timer0 Operation

The Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

20.1.1 8-BIT TIMER MODE

The Timer0 module will increment every instruction cycle, if used without a prescaler. 8-bit Timer mode is selected by clearing the TMR0CS bit of the OPTION register.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note:	The value written to the TMR0 register					
	can be adjusted, in order to account for					
	the two instruction cycle delay when					
	TMR0 is written.					

20.1.2 8-BIT COUNTER MODE

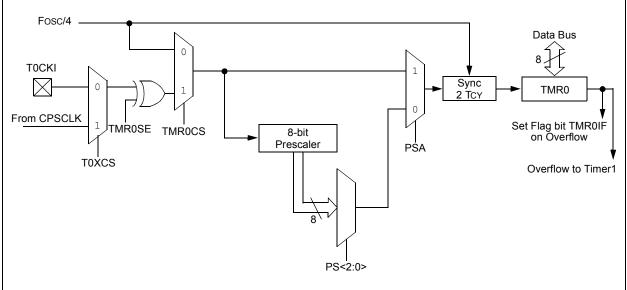
In 8-Bit Counter mode, the Timer0 module will increment on every rising or falling edge of the T0CKI pin or the Capacitive Sensing Oscillator (CPSCLK) signal.

8-Bit Counter mode using the T0CKI pin is selected by setting the TMR0CS bit in the OPTION register to '1' and resetting the T0XCS bit in the CPSCON0 register to '0'.

8-Bit Counter mode using the Capacitive Sensing Oscillator (CPSCLK) signal is selected by setting the TMR0CS bit in the OPTION register to '1' and setting the T0XCS bit in the CPSCON0 register to '1'.

The rising or falling transition of the incrementing edge for either input source is determined by the TMR0SE bit in the OPTION register.

FIGURE 20-1: BLOCK DIAGRAM OF THE TIMER0



20.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A software programmable prescaler is available for exclusive use with Timer0. The prescaler is enabled by clearing the PSA bit of the OPTION register.

Note:	The Watchdog Timer (WDT) uses its own					
	independent prescaler.					

There are 8 prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be disabled by setting the PSA bit of the OPTION register.

The prescaler is not readable or writable. All instructions writing to the TMR0 register will clear the prescaler.

20.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TMR0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TMR0IF bit can only be cleared in software. The Timer0 interrupt enable is the TMR0IE bit of the INTCON register.

Note:	The Timer0 interrupt cannot wake the					
	processor from Sleep since the timer is					
	frozen during Sleep.					

20.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in Section 30.0 "Electrical Specifications".

20.1.6 OPERATION DURING SLEEP

Timer0 cannot operate while the processor is in Sleep mode. The contents of the TMR0 register will remain unchanged while the processor is in Sleep mode.

		—								
R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1			
WPUEN	INTEDG	TMR0CS	TMR0SE	PSA		PS<2:0>				
bit 7							bit C			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'				
u = Bit is unch	nanged	x = Bit is unk	nown	-n/n = Value a	at POR and BC	R/Value at all c	ther Resets			
'1' = Bit is set		'0' = Bit is cle	eared							
bit 7		ak Pull-up Ena								
				MCLR, if it is						
bit 6	•	errupt Edge Se	•	al WPUx latch	values					
		on rising edge		n						
		on falling edge								
bit 5	-	mer0 Clock So	-							
	1 = Transitio	n on RA4/T0Cl	on RA4/T0CKI pin							
	0 = Internal i	nstruction cycle	e clock (Fosc/4	4)						
bit 4		IMR0SE: Timer0 Source Edge Select bit								
	 1 = Increment on high-to-low transition on RA4/T0CKI pin 0 = Increment on low-to-high transition on RA4/T0CKI pin 									
bit 3		ler Assignmen								
bit 5		r is not assigne		0 module						
		r is assigned to								
bit 2-0	PS<2:0>: Pre	escaler Rate S	elect bits							
	Bit	Value Timer0	Rate							
		000 1:2	2							
		001 1 :4								
		010 1:8 011 1: 1								
		100 1:3								

REGISTER 20-1: OPTION_REG: OPTION REGISTER

TABLE 20-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

1:64

1:128

1:256

101

110 111

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CPSCON0	CPSON	CPSRM	_	_	CPSRNG1	CPSRNG0	CPSOUT	TOXCS	333
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFV	′R<1:0>	ADFVF	R<1:0>	148
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
OPTION_REG	WPUEN INTEDG TMR0CS TMR0SE PSA PS<2:0>						189		
TMR0	Timer0 Module Register							187*	
TRISA	_		TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the Timer0 module. * Page provides register information. NOTES:

21.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 2-bit prescaler
- · Dedicated 32 kHz oscillator circuit
- · Optionally synchronized comparator out
- Multiple Timer1 gate (count enable) sources
- · Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Special Event Trigger (with CCP/ECCP)
- Selectable Gate Source Polarity

- Gate Toggle Mode
- Gate Single-pulse Mode
- Gate Value Status
- Gate Event Interrupt
- Figure 21-1 is a block diagram of the Timer1 module.

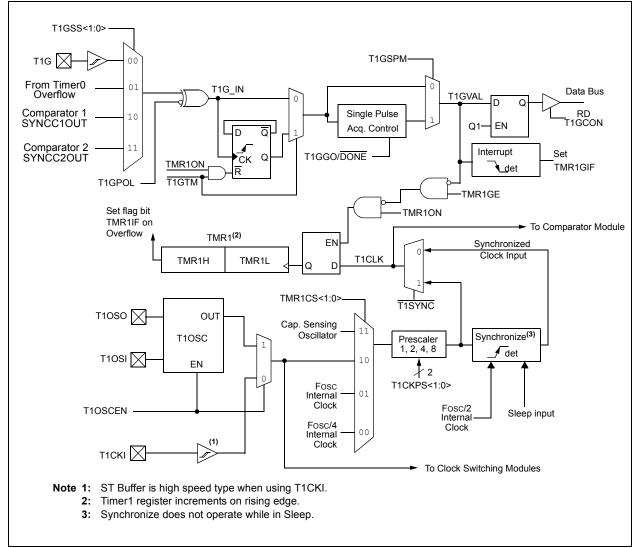


FIGURE 21-1: TIMER1 BLOCK DIAGRAM

21.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1 is enabled by configuring the TMR1ON and TMR1GE bits in the T1CON and T1GCON registers, respectively. Table 21-1 displays the Timer1 enable selections.

TABLE 21-1:	TIMER1 ENABLE
	SELECTIONS

TMR10N	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	Always On
1	1	Count Enabled

21.2 Clock Source Selection

The TMR1CS<1:0> and T1OSCEN bits of the T1CON register are used to select the clock source for Timer1. Table 21-2 displays the clock source selections.

21.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected the TMR1H:TMR1L register pair will increment on multiples of Fosc as determined by the Timer1 prescaler.

When the Fosc internal clock source is selected, the Timer1 register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the Timer1 value. To utilize the full resolution of Timer1, an asynchronous input signal must be used to gate the Timer1 clock input.

The following asynchronous sources may be used:

- Asynchronous event on the T1G pin to Timer1 Gate
- C1 or C2 comparator input to Timer1 Gate

21.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When enabled to count, Timer1 is incremented on the rising edge of the external clock input T1CKI or the capacitive sensing oscillator signal. Either of these external clock sources can be synchronized to the microcontroller system clock or they can run asynchronously.

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used in conjunction with the dedicated internal oscillator circuit.

- **Note:** In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:
 - Timer1 enabled after POR
 - Write to TMR1H or TMR1L
 - Timer1 is disabled
 - Timer1 is disabled (TMR1ON = 0) when T1CKI is high then Timer1 is enabled (TMR1ON=1) when T1CKI is low.

TMR1CS1	TMR1CS0	T1OSCEN	Clock Source
0	1	x	System Clock (Fosc)
0	0	х	Instruction Clock (Fosc/4)
1	1	х	Capacitive Sensing Oscillator
1	0	0	External Clocking on T1CKI Pin
1	0	1	Osc.Circuit On T1OSI/T1OSO Pins

TABLE 21-2: CLOCK SOURCE SELECTIONS

21.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

21.4 Timer1 Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). This internal circuit is to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the T1OSCEN bit of the T1CON register. The oscillator will continue to run during Sleep.

Note:	The oscillator requires a start-up and					
	stabilization time before use. Thus,					
	T1OSCEN should be set and a suitable					
	delay observed prior to enabling Timer1.					

21.5 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see Section 21.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode").

Note:	When switching from synchronous to
	asynchronous operation, it is possible to
	skip an increment. When switching from
	asynchronous to synchronous operation,
	it is possible to produce an additional
	increment.

21.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

21.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 Gate circuitry. This is also referred to as Timer1 Gate Enable.

Timer1 Gate can also be driven by multiple selectable sources.

21.6.1 TIMER1 GATE ENABLE

The Timer1 Gate Enable mode is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 21-3 for timing details.

TABLE 21-3:TIMER1 GATE ENABLESELECTIONS

T1CLK	T1GPOL	T1G Timer1 Operation			
\uparrow	0	0	Counts		
\uparrow	0	1	Holds Count		
\uparrow	1	0	Holds Count		
\uparrow	1	1	Counts		

21.6.2 TIMER1 GATE SOURCE SELECTION

The Timer1 Gate source can be selected from one of four different sources. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

TABLE 21-4: TIMER1 GATE SOURCES

T1GSS	Timer1 Gate Source
00	Timer1 Gate Pin
01	Overflow of Timer0 (TMR0 increments from FFh to 00h)
10	Comparator 1 Output SYNCC1OUT (optionally Timer1 synchronized output)
11	Comparator 2 Output SYNCC2OUT (optionally Timer1 synchronized output)

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21.6.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 Gate Control. It can be used to supply an external source to the Timer1 Gate circuitry.

21.6.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 Gate circuitry.

21.6.2.3 Comparator C1 Gate Operation

The output resulting from a Comparator 1 operation can be selected as a source for Timer1 Gate Control. The Comparator 1 output (SYNCC1OUT) can be synchronized to the Timer1 clock or left asynchronous. For more information see Section 19.4.1 "Comparator Output Synchronization".

21.6.2.4 Comparator C2 Gate Operation

The output resulting from a Comparator 2 operation can be selected as a source for Timer1 Gate Control. The Comparator 2 output (SYNCC2OUT) can be synchronized to the Timer1 clock or left asynchronous. For more information see Section 19.4.1 "Comparator Output Synchronization".

21.6.3 TIMER1 GATE TOGGLE MODE

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 Gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 21-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note:	Enabling Toggle mode at the same time					
	as changing the gate polarity may result in					
	indeterminate operation.					

21.6.4 TIMER1 GATE SINGLE-PULSE MODE

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer1 Gate Single-Pulse mode is first enabled by setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/DONE bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/DONE bit is once again set in software. See Figure 21-5 for timing details.

If the Single Pulse Gate mode is disabled by clearing the T1GSPM bit in the T1GCON register, the T1GGO/DONE bit should also be cleared.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 Gate source to be measured. See Figure 21-6 for timing details.

21.6.5 TIMER1 GATE VALUE STATUS

When Timer1 Gate Value Status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 Gate is not enabled (TMR1GE bit is cleared).

21.6.6 TIMER1 GATE EVENT INTERRUPT

When Timer1 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T1GVAL occurs, the TMR1GIF flag bit in the PIR1 register will be set. If the TMR1GIE bit in the PIE1 register is set, then an interrupt will be recognized.

The TMR1GIF flag bit operates even when the Timer1 Gate is not enabled (TMR1GE bit is cleared).

21.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR1ON bit of the T1CON register
- TMR1IE bit of the PIE1 register
- · PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note: The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

21.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set
- T1SYNC bit of the T1CON register must be set
- TMR1CS bits of the T1CON register must be configured
- T1OSCEN bit of the T1CON register must be configured

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine.

Timer1 oscillator will continue to operate in Sleep regardless of the T1SYNC bit setting.

21.9 ECCP/CCP Capture/Compare Time Base

The CCP modules use the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see Section 24.0 "Capture/Compare/PWM Modules".

21.10 ECCP/CCP Special Event Trigger

When any of the CCP's are configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair becomes the period register for Timer1.

Timer1 should be synchronized and Fosc/4 should be selected as the clock source in order to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the CCP, the write will take precedence.

For more information, see **Section 16.2.5** "Special **Event Trigger**".

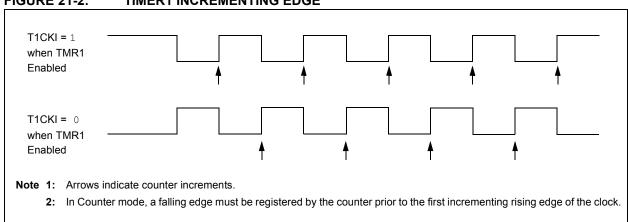


FIGURE 21-2: TIMER1 INCREMENTING EDGE

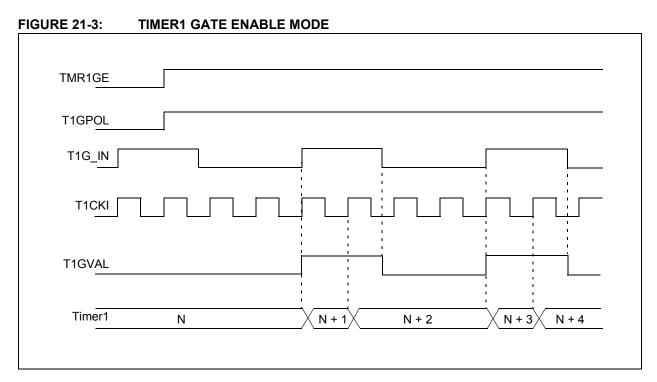


FIGURE 21-4: TIMER1 GATE TOGGLE MODE

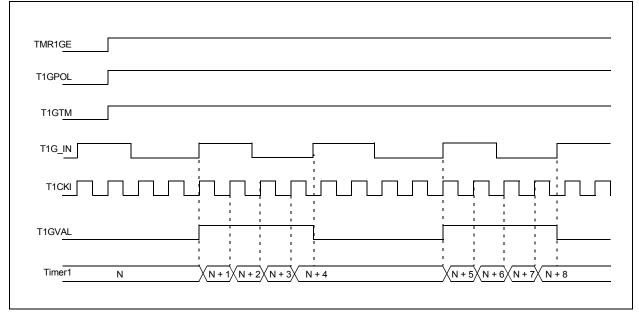
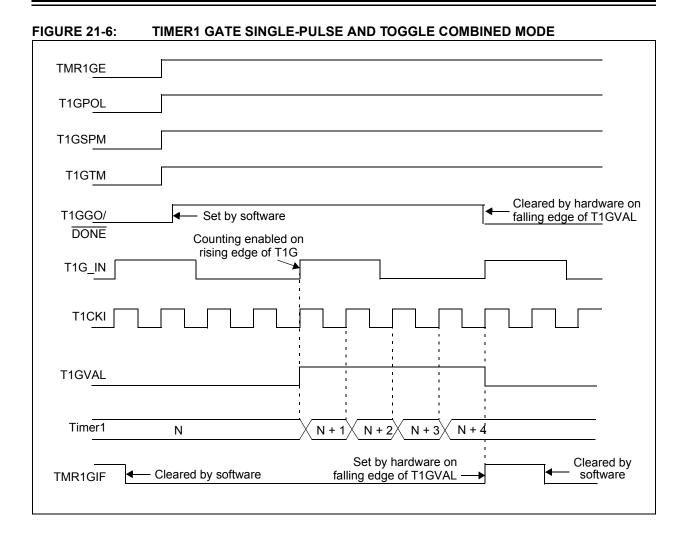


FIGURE 21-5:	TIMER1 GATE SINGLE-	PULSE MODE	
TMR1GE			
T1GPOL			
T1GSPM			
T1GG <u>O/</u> DONE	▲ Set by software Counting enabled of	n	Cleared by hardware on falling edge of T1GVAL
T1G_IN	rising edge of T10	A	
т1СКІ			
T1GV <u>AL</u>			
Timer1	Ν	<u>N + 1</u>	N + 2
TMR1GIF	Cleared by software		Set by hardware on falling edge of T1GVAL



21.11 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 21-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 21-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	U-0	R/W-0/u
TMR1C	S<1:0>	T1CKPS<1:0>		T1OSCEN	T1SYNC	—	TMR10N
bit 7						bit 0	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	TMR1CS<1:0>: Timer1 Clock Source Select bits
	11 = Timer1 clock source is Capacitive Sensing Oscillator (CAPOSC)
	10 = Timer1 clock source is pin or oscillator:
	$\frac{\text{If T1OSCEN} = 0}{\text{If T1OSCEN}}$
	External clock from T1CKI pin (on the rising edge)
	<u>If T1OSCEN = 1</u> : Crystal oscillator on T1OSI/T1OSO pins
	01 = Timer1 clock source is system clock (Fosc)
	00 = Timer1 clock source is instruction clock (Fosc/4)
bit 5-4	T1CKPS<1:0>: Timer1 Input Clock Prescale Select bits
	11 = 1:8 Prescale value
	10 = 1:4 Prescale value
	01 = 1:2 Prescale value
	00 = 1:1 Prescale value
bit 3	T10SCEN: LP Oscillator Enable Control bit
	1 = Dedicated Timer1 oscillator circuit enabled
	0 = Dedicated Timer1 oscillator circuit disabled
bit 2	T1SYNC: Timer1 External Clock Input Synchronization Control bit
	$\underline{TMR1CS} = 1X$
	1 = Do not synchronize external clock input
	0 = Synchronize external clock input with system clock (Fosc)
	$\underline{TMR1CS} = 0X$
	This bit is ignored. Timer1 uses the internal clock when TMR1CS<1:0> = 1x.
bit 1	Unimplemented: Read as '0'
bit 0	TMR1ON: Timer1 On bit
	1 = Enables Timer1
	0 = Stops Timer1
	Clears Timer1 Gate flip-flop

21.12 Timer1 Gate Control Register

The Timer1 Gate Control register (T1GCON), shown in Register 21-2, is used to control Timer1 Gate.

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W/HC-0/u	R-x/x	R/W-0/u	R/W-0/u
TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/ DONE	T1GVAL	T1GS	S<1:0>
bit 7		·	·				bit (
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
u = Bit is uncl	hanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is clea	ared	HC = Bit is cle	eared by hardw	/are	
bit 7	If TMR1ON = This bit is ign If TMR1ON = 1 = Timer1 c	ored <u>1</u> :	rolled by the Ti	imer1 gate func	tion		
bit 6	1 = Timer1 g	T1GPOL: Timer1 Gate Polarity bit 1 = Timer1 gate is active-high (Timer1 counts when gate is high) 0 = Timer1 gate is active-low (Timer1 counts when gate is low)					
bit 5	1 = Timer1 G 0 = Timer1 G	 T1GTM: Timer1 Gate Toggle Mode bit 1 = Timer1 Gate Toggle mode is enabled 0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared Timer1 gate flip-flop toggles on every rising edge. 					
bit 4	1 = Timer1 g	TIGSPM: Timer1 Gate Single-Pulse Mode bit 1 = Timer1 gate Single-Pulse mode is enabled and is controlling Timer1 gate 0 = Timer1 gate Single-Pulse mode is disabled					
bit 3	T1GGO/DON 1 = Timer1 g	 TIGGO/DONE: Timer1 Gate Single-Pulse Acquisition Status bit 1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge 0 = Timer1 gate single-pulse acquisition has completed or has not been started 					
bit 2	T1GVAL: Timer1 Gate Current State bit Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L. Unaffected by Timer1 Gate Enable (TMR1GE).						
bit 1-0							

REGISTER 21-2: T1GCON: TIMER1 GATE CONTROL REGISTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	_	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	130
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	240
CCP2CON	P2M1	P2M0	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	240
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
TMR1H	Holding Regist	er for the Most	Significant Byte	of the 16-bit T	MR1 Register				195*
TMR1L	Holding Regist	er for the Least	Significant Byte	e of the 16-bit 1	FMR1 Register				195*
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
T1CON	TMR1CS1	TMR1CS0	T1CKP	S<1:0>	T1OSCEN	T1SYNC	_	TMR10N	199
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T <u>1GGO</u> / DONE	T1GVAL	T1GSS1	T1GSS0	200

TABLE 21-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

— = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module. Page provides register information. Legend:

NOTES:

22.0 TIMER2/4/6 MODULES

There are up to three identical Timer2-type modules available. To maintain pre-existing naming conventions, the Timers are called Timer2, Timer4 and Timer6 (also Timer2/4/6).

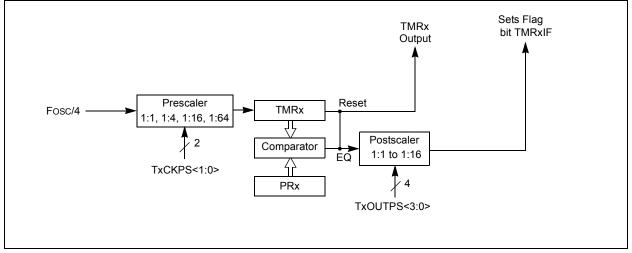
Note:	The 'x' variable used in this section is used to designate Timer2, Timer4 or Timer6. For example, TxCON references T2CON, T4CON or T6CON. PRx refer-
	ences PR2, PR4 or PR6.

The Timer2/4/6 modules incorporate the following features:

- 8-bit Timer and Period registers (TMRx and PRx, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16, and 1:64)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMRx match with PRx, respectively
- Optional use as the shift clock for the MSSPx modules (Timer2 only)

See Figure 22-1 for a block diagram of Timer2/4/6.

FIGURE 22-1: TIMER2/4/6 BLOCK DIAGRAM



22.1 Timer2/4/6 Operation

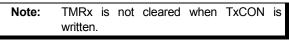
The clock input to the Timer2/4/6 modules is the system instruction clock (Fosc/4).

TMRx increments from 00h on each clock edge.

A 4-bit counter/prescaler on the clock input allows direct input, divide-by-4 and divide-by-16 prescale options. These options are selected by the prescaler control bits, TxCKPS<1:0> of the TxCON register. The value of TMRx is compared to that of the Period register, PRx, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMRx to 00h on the next cycle and drives the output counter/postscaler (see Section 22.2 "Timer2/4/6 Interrupt").

The TMRx and PRx registers are both directly readable and writable. The TMRx register is cleared on any device Reset, whereas the PRx register initializes to FFh. Both the prescaler and postscaler counters are cleared on the following events:

- · a write to the TMRx register
- · a write to the TxCON register
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- MCLR Reset
- Watchdog Timer (WDT) Reset
- · Stack Overflow Reset
- · Stack Underflow Reset
- RESET Instruction



22.2 Timer2/4/6 Interrupt

Timer2/4/6 can also generate an optional device interrupt. The Timer2/4/6 output signal (TMRx-to-PRx match) provides the input for the 4-bit counter/postscaler. This counter generates the TMRx match interrupt flag which is latched in TMRxIF of the PIRx register. The interrupt is enabled by setting the TMRx Match Interrupt Enable bit, TMRxIE of the PIEx register.

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, TxOUTPS<3:0>, of the TxCON register.

22.3 Timer2/4/6 Output

The unscaled output of TMRx is available primarily to the CCP modules, where it is used as a time base for operations in PWM mode.

Timer2 can be optionally used as the shift clock source for the MSSPx modules operating in SPI mode. Additional information is provided in Section 25.0 "Master Synchronous Serial Port (MSSP1 and MSSP2) Module".

22.4 Timer2/4/6 Operation During Sleep

The Timer2/4/6 timers cannot be operated while the processor is in Sleep mode. The contents of the TMRx and PRx registers will remain unchanged while the processor is in Sleep mode.

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0			
—		TxOUTF	PS<3:0>		TMRxON	TxCKP	'S<1:0>			
bit 7							bit			
Legend:										
R = Readal	ble bit	W = Writable	bit	U = Unimple	mented bit, read	l as '0'				
u = Bit is ur		x = Bit is unkr	nown	-	at POR and BO		other Resets			
'1' = Bit is s	•	'0' = Bit is clea	ared							
L:4 7		utada Daadaa (~ '							
bit 7	-	ented: Read as '								
bit 6-3		3:0>: Timerx Ou	tput Postscale	er Select bits						
		0000 = 1:1 Postscaler								
	0001 = 1:2 Postscaler 0010 = 1:3 Postscaler									
		0011 = 1:4 Postscaler								
		0100 = 1:5 Postscaler								
		0101 = 1:6 Postscaler								
	0110 = 1:7	0110 = 1:7 Postscaler								
		11 = 1:8 Postscaler								
	1000 = 1:9									
	1001 = 1:10									
	1010 = 1:11 Postscaler									
	1011 = 1:12 Postscaler 1100 = 1:13 Postscaler									
		1100 = 1.13 Postscaler $1101 = 1.14 Postscaler$								
		1110 = 1:15 Postscaler								
	1111 = 1:16 Postscaler									
bit 2	TMRxON: 7									
	1 = Timerx	is on								
	0 = Timerx is off									
bit 1-0	TxCKPS<1	:0>: Timer2-type	Clock Presca	ale Select bits						
	00 = Presca	aler is 1								
	01 = Presca	aler is 4								
	10 = Presca	aler is 16								

REGISTER 22-1: TXCON: TIMER2/TIMER4/TIMER6 CONTROL REGISTER

Name	Bit 7	Bit 6	Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0							
CCP2CON	P2M1	P2M0	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	240	
CCP4CON	—		DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	240	
CCP6CON	—		DC6B1	DC6B0	CCP6M3	CCP6M2	CCP6M1	CCP6M0	240	
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93	
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94	
PIE3	—	-	- CCP4IE CCP3IE TMR6IE - TMR4IE -							
PIR1	TMR1GIF	ADIF	ADIF RCIF TXIF SSP1IF CCP1IF TMR2IF TMR1IF						98	
PIR3	—	-	- CCP4IF CCP3IF TMR6IF - TMR4IF -							
PR2	Timer2 Mod	dule Period	Register						203*	
PR4	Timer4 Mod	dule Period	Register						203*	
PR6	Timer6 Mod	dule Period	Register						203*	
T2CON	—		T2OUTF	PS<3:0>		TMR2ON	T2CKPS1	T2CKPS0	205	
T4CON	—		T4OUTF	PS<3:0>		TMR4ON	T4CKPS1	T4CKPS0	205	
T6CON	- T6OUTPS<3:0> TMR6ON T6CKPS1 T6CKPS0									
TMR2	Holding Register for the 8-bit TMR2 Register								203*	
TMR4	Holding Register for the 8-bit TMR4 Register ⁽¹⁾									
TMR6	Holding Re	gister for the	e 8-bit TMR6	8 Register ⁽¹⁾)				203*	

TABLE 22-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2/4/6

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2/4/6 module.

* Page provides register information.

23.0 DATA SIGNAL MODULATOR

The Data Signal Modulator (DSM) is a peripheral which allows the user to mix a data stream, also known as a modulator signal, with a carrier signal to produce a modulated output.

Both the carrier and the modulator signals are supplied to the DSM module either internally, from the output of a peripheral, or externally through an input pin.

The modulated output signal is generated by performing a logical "AND" operation of both the carrier and modulator signals and then provided to the MDOUT pin.

The carrier signal is comprised of two distinct and separate signals. A carrier high (CARH) signal and a carrier low (CARL) signal. During the time in which the modulator (MOD) signal is in a logic high state, the DSM mixes the carrier high signal with the modulator signal. When the modulator signal is in a logic low state, the DSM mixes the carrier low signal with the modulator signal. Using this method, the DSM can generate the following types of Key Modulation schemes:

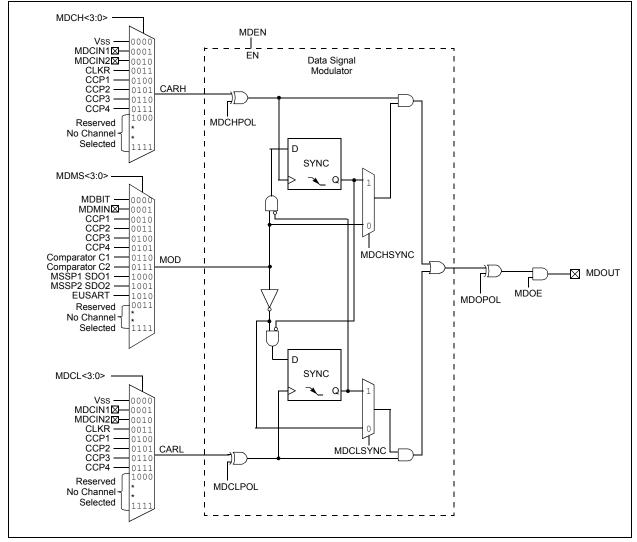
- Frequency-Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Additionally, the following features are provided within the DSM module:

- Carrier Synchronization
- · Carrier Source Polarity Select
- Carrier Source Pin Disable
- Programmable Modulator Data
- Modulator Source Pin Disable
- Modulated Output Polarity Select
- Slew Rate Control

Figure 23-1 shows a Simplified Block Diagram of the Data Signal Modulator peripheral.





23.1 DSM Operation

The DSM module can be enabled by setting the MDEN bit in the MDCON register. Clearing the MDEN bit in the MDCON register, disables the DSM module by automatically switching the carrier high and carrier low signals to the Vss signal source. The modulator signal source is also switched to the MDBIT in the MDCON register. This not only assures that the DSM module is inactive, but that it is also consuming the least amount of current.

The values used to select the carrier high, carrier low, and modulator sources held by the Modulation Source, Modulation High Carrier, and Modulation Low Carrier control registers are not affected when the MDEN bit is cleared and the DSM module is disabled. The values inside these registers remain unchanged while the DSM is inactive. The sources for the carrier high, carrier low and modulator signals will once again be selected when the MDEN bit is set and the DSM module is again enabled and active.

The modulated output signal can be disabled without shutting down the DSM module. The DSM module will remain active and continue to mix signals, but the output value will not be sent to the MDOUT pin. During the time that the output is disabled, the MDOUT pin will remain low. The modulated output can be disabled by clearing the MDOE bit in the MDCON register.

23.2 Modulator Signal Sources

The modulator signal can be supplied from the following sources:

- CCP1 Signal
- CCP2 Signal
- CCP3 Signal
- CCP4 Signal
- MSSP1 SDO1 Signal (SPI Mode Only)
- MSSP2 SDO2 Signal (SPI Mode Only)
- · Comparator C1 Signal
- · Comparator C2 Signal
- EUSART TX Signal
- External Signal on MDMIN pin
- MDBIT bit in the MDCON register

The modulator signal is selected by configuring the MDMS <3:0> bits in the MDSRC register.

23.3 Carrier Signal Sources

The carrier high signal and carrier low signal can be supplied from the following sources:

- CCP1 Signal
- CCP2 Signal
- CCP3 Signal
- CCP4 Signal
- Reference Clock Module Signal
- External Signal on MDCIN1 pin
- External Signal on MDCIN2 pin
- Vss

The carrier high signal is selected by configuring the MDCH <3:0> bits in the MDCARH register. The carrier low signal is selected by configuring the MDCL <3:0> bits in the MDCARL register.

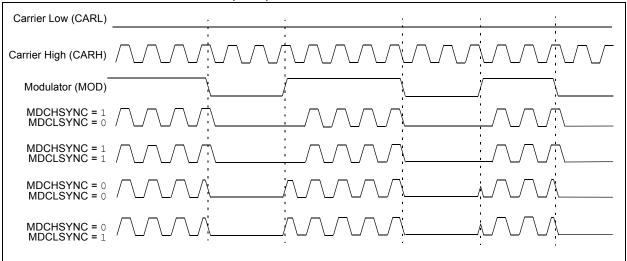
23.4 Carrier Synchronization

During the time when the DSM switches between carrier high and carrier low signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the modulator signal. When synchronization is enabled, the carrier pulse that is being mixed at the time of the transition is allowed to transition low before the DSM switches over to the next carrier source.

Synchronization is enabled separately for the carrier high and carrier low signal sources. Synchronization for the carrier high signal can be enabled by setting the MDCHSYNC bit in the MDCARH register. Synchronization for the carrier low signal can be enabled by setting the MDCLSYNC bit in the MDCARL register.

Figure 23-1 through Figure 23-5 show timing diagrams of using various synchronization methods.

FIGURE 23-2: ON OFF KEYING (OOK) SYNCHRONIZATION



EXAMPLE 23-1: NO SYNCHRONIZATION (MDSHSYNC = 0, MDCLSYNC = 0)

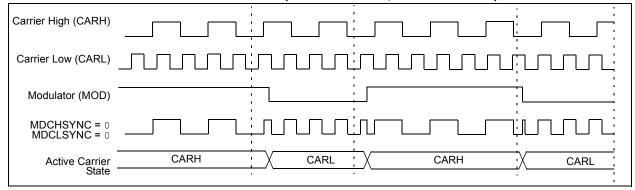
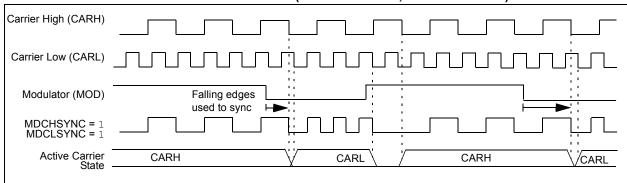


FIGURE 23-3: CARRIER HIGH SYNCHRONIZATION (MDSHSYNC = 1, MDCLSYNC = 0)

Carrier High (CARH)	
Carrier Low (CARL)	
Modulator (MOD)	
MDCHSYNC = 1 MDCLSYNC = 0	
Active Carrier State	CARH / both CARL / CARH / both CARL

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FIGURE 23-4:	CARRIER LOW SYNCHRONIZATION (MDSHSYNC = 0, MDCLSYNC = 1)
Carrier High (CARH)	
Carrier Low (CARL)	
Modulator (MOD)	
MDCHSYNC = 0 MDCLSYNC = 1	
Active Carrier State -	
FIGURE 23-5:	FULL SYNCHRONIZATION (MDSHSYNC = 1, MDCLSYNC = 1)



23.5 CARRIER SOURCE POLARITY SELECT

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the MDCHPOL bit of the MDCARH register. Inverting the signal for the carrier low source is enabled by setting the MDCLPOL bit of the MDCARL register.

23.6 CARRIER SOURCE PIN DISABLE

Some peripherals assert control over their corresponding output pin when they are enabled. For example, when the CCP1 module is enabled, the output of CCP1 is connected to the CCP1 pin.

This default connection to a pin can be disabled by setting the MDCHODIS bit in the MDCARH register for the carrier high source and the MDCLODIS bit in the MDCARL register for the carrier low source.

23.7 PROGRAMMABLE MODULATOR DATA

The MDBIT of the MDCON register can be selected as the source for the modulator signal. This gives the user the ability to program the value used for modulation.

23.8 MODULATOR SOURCE PIN DISABLE

The modulator source default connection to a pin can be disabled by setting the MDMSODIS bit in the MDSRC register.

23.9 MODULATED OUTPUT POLARITY

The modulated output signal provided on the MDOUT pin can also be inverted. Inverting the modulated output signal is enabled by setting the MDOPOL bit of the MDCON register.

23.10 SLEW RATE CONTROL

The slew rate limitation on the output port pin can be disabled. The slew rate limitation can be removed by clearing the MDSLR bit in the MDCON register.

23.11 OPERATION IN SLEEP MODE

The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep.

23.12 Effects of a Reset

Upon any device Reset, the data signal modulator module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

R/W-0	/0 R/W-0/0	R/W-1/1	R/W-0/0	R-0/0	U-0	U-0	R/W-0/0
MDE	N MDOE	MDSLR	MDOPOL	MDOUT	—	_	MDBIT
bit 7							bit 0
Legend: R = Read	abla bit		L:1			aa (0)	
		W = Writable		•	mented bit, read at POR and BOF		athar Daaata
	unchanged	x = Bit is unk			at POR and BOR	value at all o	Siner Reseis
'1' = Bit is	set	'0' = Bit is cle	ared				
bit 7	MDEN: Mod	lulator Module E	nable bit				
	1 = Modula	tor module is er	abled and mix	ing input signa	als		
		tor module is dis		• • •			
bit 6	MDOE: Mod	dulator Module F	Pin Output Ena	ıble bit			
		tor pin output er					
	0 = Modula	tor pin output di	sabled				
bit 5		DOUT Pin Slew	0				
		Γ pin slew rate li Γ pin slew rate li	Ų				
bit 4		Modulator Outpu	•				
DIL 4		tor output signa					
		tor output signa		d			
bit 3		odulator Output					
		current output		odulator modu	ıle. ⁽¹⁾		
bit 2-1	Unimpleme	nted: Read as	0'				
bit 0	MDBIT: Allo	ws software to r	nanually set m	odulation sou	rce input to mod	ule ⁽²⁾	
		tor uses High C	-				
	0 = Modula	tor uses Low Ca	arrier source				
Note 1:	The modulated o						ates this
	register bit, the b	it value may not	be valid for hi	gher speed m	odulator or carrie	er signals.	

REGISTER 23-1: MDCON: MODULATION CONTROL REGISTER

2: MDBIT must be selected as the modulation source in the MDSRC register for this operation.

it 7 bit eegend: R R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets 1' = Bit is set '0' = Bit is cleared it 7 MDMSODIS: Modulation Source Output Disable bit 1 = Output signal driving the peripheral output pin (selected by MDMS<3:0>) is disabled 0 = Output signal driving the peripheral output pin (selected by MDMS<3:0>) is enabled it 6-4 Unimplemented: Read as '0'	R/W-x/u	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
egend: Readable bit W = Writable bit U = Unimplemented bit, read as '0' = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets I' = Bit is set '0' = Bit is cleared it 7 MDMSODIS: Modulation Source Output Disable bit 1 = Output signal driving the peripheral output pin (selected by MDMS<3:0>) is disabled 0 = Output signal driving the peripheral output pin (selected by MDMS<3:0>) is enabled it 6-4 Unimplemented: Read as '0' it 3-0 MDMS<3:0> Modulation Source Selection bits 1111 = Reserved. No channel connected. 1101 = Reserved. No channel connected. 1100 = Reserved. No channel connected. 100 = Reserved. No channel connected. 1011 = Reserved. No channel connected. 101 = Reserved. No channel connected. 1010 = EUSART TX output 1001 = MSSP1 SDOx output 1001 = MSSP1 SDOx output 0101 = Comparator1 output 0101 = CCP4 output (PWM Output mode only) 0101 = CCP3 output (PWM Output mode only) 0101 = CCP2 output (PWM Output mode only) 0101 = CCP2 output (PWM Output mode only) 0101 = CCP1 output (PWM Output mode only) 001 = CCP1 output (PWM Output mode only) 0010 = CCP1 output (PWM Output mode only) 0011 = CCP1 output (PWM Output mode only) <td>MDMSODIS</td> <td>—</td> <td>—</td> <td>_</td> <td></td> <td>MDMS</td> <td>S<3:0></td> <td></td>	MDMSODIS	—	—	_		MDMS	S<3:0>	
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0010 = CCP1 output (PWM Output mode only) 0001 = MDMIN port pin								
0001 = MDMIN port pin								
					ie only)			
UUUU = MIDBIT DIL OF MIDCON register is modulation source				NI register :-	modulation	1700		
		0000 = ML		JN register is	s modulation sol	lice		

REGISTER 23-2: MDSRC: MODULATION SOURCE CONTROL REGISTER

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

R/W-x/u	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
MDCHODIS	MDCHPOL	MDCHSYNC	_		MDCH	1<3:0>	
bit 7				·			bit 0
Logondi							
Legend: R = Readable I	nit	W = Writable bit		II – Unimplen	nented bit, read	l ac 'O'	
u = Bit is uncha		x = Bit is unknown			at POR and BO		thar Basata
	angeu				at FOR and BO	rv value at all t	
'1' = Bit is set		'0' = Bit is cleare	ea				
bit 7	MDCHODIS	Modulator High (Carrier Out	nut Disable bit			
bit i		ignal driving the p		•	ted by MDCH<	3·0>) is disable	≏d
		ignal driving the p					
bit 6	MDCHPOL:	Modulator High C	arrier Pola	rity Select bit	-		
	1 = Selected	I high carrier signa	al is inverte	ed			
	0 = Selected	I high carrier signa	al is not in	verted			
bit 5	MDCHSYNC	: Modulator High	Carrier Sy	nchronization Er	nable bit		
	1 = Modulate	or waits for a fallin	ng edge oi	n the high time o	arrier signal be	efore allowing	a switch to the
	low time			11.0.11.0.0		(1)	
		or Output is not sy	/ncnronize	a to the high tim	e carrier signal	(')	
bit 4	•	nted: Read as '0'		,	4		
bit 3-0		Modulator Data H			(1)		
	1111 = Res	erved. No chann	el connect	ed.			
	•						
	•						
	1000 = Res	erved. No chann	el connect	ed.			
		P4 output (PWM 0					
		P3 output (PWM (
		P2 output (PWM 0 P1 output (PWM 0					
		erence Clock mod					
	0010 = MD(iaio orginal				
	0001 = MD0						
	0000 = Vss						

REGISTER 23-3: MDCARH: MODULATION HIGH CARRIER CONTROL REGISTER

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

R/W-x/u	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
MDCLODIS	MDCLPOL	MDCLSYNC	_		MDCL	_<3:0>	
bit 7							bit 0
Lawawak							
Legend: R = Readable	hit.	M = Mritabla b	.:+		nantad hit raad	l aa 'O'	
		W = Writable b			nented bit, read at POR and BO		athar Daaata
u = Bit is unch	angeu	x = Bit is unknown				R/value at all o	Siner Reseis
'1' = Bit is set		'0' = Bit is clea	rea				
bit 7		Modulator Low	Carrier Out	out Disable bit			
		signal driving the			ted by MDCI <3	0> of the MD	CARL register
	is disable		periprierary				
		ignal driving the	peripheral of	output pin (selec	ted by MDCL<3	:0> of the MD	CARL register)
	is enable						
bit 6		Modulator Low C		•			
		d low carrier sign d low carrier sign					
bit 5		: Modulator Low			ahle hit		
bit b		or waits for a falli	-			e allowing a sw	itch to the hiah
	time carı	rier			-	-	
	0 = Modulate	or Output is not s	synchronize	d to the low time	e carrier signal ⁽¹	1)	
bit 4	-	nted: Read as '0					
bit 3-0		Modulator Data	•		(1)		
	1111 = Res	served. No chan	nel connect	ed.			
	•						
	•						
		erved. No chan					
		P4 output (PWM					
		P3 output (PWM P2 output (PWM					
		P1 output (PWM					
		erence Clock mo	dule signal				
		CIN2 port pin					
	0001 = MD00000 = Vss	CIN1 port pin					

REGISTER 23-4: MDCARL: MODULATION LOW CARRIER CONTROL REGISTER

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
MDCARH	MDCHODIS	MDCHPOL	MDCHSYNC	—		MDCH<3:0>		214	
MDCARL	MDCLODIS	MDCLPOL	MDCLSYNC	_		MDCL<3:0>			215
MDCON	MDEN	MDOE	MDSLR	MDOPOL	MDOUT MDBIT		212		
MDSRC	MDMSODIS	_	—	—	MDMS<3:0>		213		

Legend: — = unimplemented, read as '0'. Shaded cells are not used in the Data Signal Modulator mode.

NOTES:

24.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

This family of devices contains two Enhanced Capture/ Compare/PWM modules (ECCP1 and ECCP2) and two standard Capture/Compare/PWM modules (CCP3 and CCP4).

The Capture and Compare functions are identical for all four CCP modules (ECCP1, ECCP2, CCP3 and CCP4). The only differences between CCP modules are in the Pulse-Width Modulation (PWM) function. The standard PWM function is identical in modules, CCP3 and CCP4. In CCP modules ECCP1 and ECCP2, the Enhanced PWM function has slight variations from one another. Full-Bridge ECCP modules have four available I/O pins while Half-Bridge ECCP modules only have two available I/O pins. See Table 24-1 for more information.

- Note 1: In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.
 - 2: Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to ECCP1, ECCP2, CCP3 and CCP4. Register names, module signals, I/O pins, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module, when required.

TABLE 24-1:PWM RESOURCES

Device Name	ECCP1	ECCP2	CCP3	CCP4
PIC16F/LF1825/1829	Enhanced PWM Full-Bridge	Enhanced PWM Half-Bridge	Standard PWM	Standard PWM

24.1 Capture Mode

The Capture mode function described in this section is available and identical for CCP modules ECCP1, ECCP2, CCP3 and CCP4.

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the CCPx pin, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxM<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 24-1 shows a simplified diagram of the Capture operation.

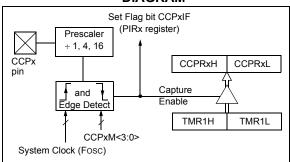
24.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Also, the CCPx pin function can be moved to alternative pins using the APFCON0 or APFCON1 register. Refer to **Section 12.1** "Alternate Pin Function" for more details.

Note: If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 24-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



24.1.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See Section 21.0 "Timer1 Module with Gate Control" for more information on configuring Timer1.

24.1.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIEx register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIRx register following any change in Operating mode.

Note:	Clocking Timer1 from the system clock
	(Fosc) should not be used in Capture
	mode. In order for Capture mode to
	recognize the trigger event on the CCPx
	pin, Timer1 must be clocked from the
	instruction clock (Fosc/4) or from an
	external clock source.

24.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCPxM<3:0> bits of the CCPxCON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler. Equation 24-1 demonstrates the code to perform this function.

EXAMPLE 24-1: CHANGING BETWEEN CAPTURE PRESCALERS

;Set Bank bits to point
;to CCPxCON
;Turn CCP module off
S;Load the W reg with
;the new prescaler
;move value and CCP ON
;Load CCPxCON with this
;value

24.1.5 CAPTURE DURING SLEEP

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock (FOSC/4), or by an external clock source.

When Timer1 is clocked by FOSC/4, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state.

Capture mode will operate during Sleep when Timer1 is clocked by an external clock source.

24.1.6 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function registers, APFCON0 and APFCON1. To determine which pins can be moved and what their default locations are upon a Reset, see Section 12.1 "Alternate Pin Function" for more information.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	-	—	SDO2SEL ⁽²⁾	SS2SEL ⁽²⁾	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	126
CCP1CON	P1M<	1:0> (1)	DC1B	<1:0>		CCP1M<	:3:0>		240
CCP2CON	P2M<	1:0> ⁽¹⁾	DC2B	<1:0>		CCP2M<	240		
CCP3CON	-	-	DC3B	<1:0>		CCP3M<	:3:0>		240
CCP4CON	-	-	DC4B	<1:0>		CCP4M<	:3:0>		240
CCPRxL	Capture/Com	pare/PWM Reg	gister x Low By	rte (LSB)					218*
CCPRxH	Capture/Com	pare/PWM Reg	gister x High B	yte (MSB)					
CMxCON0	CxON	CxOUT	CxOE	CxPOL	_	CxSP	CxHYS	CxSYNC	184
CMxCON1	CxINTP	CxINTN	CxPCH1	CxPCH0	_	-	CxNCH1	CxNCH0	185
INLVLA	-	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLC	INLVLC7(2)	INLVLC6(2)	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	_	CCP2IE	95
PIE3	_	_	CCP4IE	CCP3IE	TMR6IE	_	TMR4IE	_	96
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	99
PIR3	_	_	CCP4IF	CCP3IF	TMR6IF	_	TMR4IF	_	100
T1CON	TMR1C	S<1:0>	T1CKP	S<1:0>	T1OSCEN	T1SYNC	—	TMR10N	199
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/DONE	T1GVAL	T1GS	S<1:0>	200
TMR1L	Holding Regis	ster for the Lea	st Significant E	Byte of the 16-b	bit TMR1 Register				205*
TMR1H	Holding Regis	ster for the Mos	st Significant B	yte of the 16-b	it TMR1 Register				205*
TRISA	_	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISC	TRISC7 ⁽²⁾	TRISC6 ⁽²⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140

 TABLE 24-2:
 SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by Capture mode.

Note 1: Applies to ECCP modules only.

2: PIC16F/LF1829 only.

Page provides register information.

24.2 Compare Mode

The Compare mode function described in this section is available and identical for CCP modules ECCP1, ECCP2, CCP3 and CCP4.

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCPRxH:CCPRxL register pair is constantly compared against the 16-bit value of the TMR1H:TMR1L register pair. When a match occurs, one of the following events can occur:

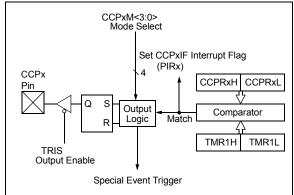
- Toggle the CCPx output
- · Set the CCPx output
- · Clear the CCPx output
- · Generate a Special Event Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCPxM<3:0> control bits of the CCPxCON register. At the same time, the interrupt flag CCPxIF bit is set.

All Compare modes can generate an interrupt.

Figure 24-2 shows a simplified diagram of the Compare operation.

FIGURE 24-2: COMPARE MODE OPERATION BLOCK DIAGRAM



24.2.1 CCP PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

Also, the CCPx pin function can be moved to alternative pins using the APFCON0 or APFCON1 register. Refer to **Section 12.1** "Alternate Pin Function" for more details.

Note:	Clearing the CCPxCON register will force
	the CCPx compare output latch to the
	default low level. This is not the PORT I/O
	data latch.

24.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See Section 21.0 "Timer1 Module with Gate Control" for more information on configuring Timer1.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, TImer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

24.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the CCPx module does not assert control of the CCPx pin (see the CCPxCON register).

24.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCPxM<3:0> = 1011), the CCPx module does the following:

- Resets Timer1
- · Starts an ADC conversion if ADC is enabled

The CCPx module does not assert control of the CCPx pin in this mode.

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPRxH, CCPRxL register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. The Special Event Trigger output starts an A/D conversion (if the A/D module is enabled). This allows the CCPRxH, CCPRxL register pair to effectively provide a 16-bit programmable period register for Timer1.

TABLE 24-3: SPECIAL EVENT TRIGGER

Device	CCPx/ECCPx
PIC16F/LF1825/1829	CCP4

Refer to Section 16.2.5 "Special Event Trigger" for more information.

- Note 1: The Special Event Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.
 - 2: Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

24.2.5 COMPARE DURING SLEEP

The Compare mode is dependent upon the system clock (Fosc) for proper operation. Since Fosc is shut down during Sleep mode, the Compare mode will not function properly during Sleep.

24.2.6 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function registers, APFCON0 and APFCON1. To determine which pins can be moved and what their default locations are upon a Reset, see Section 12.1 "Alternate Pin Function" for more information.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	-	—	SDO2SEL ⁽²⁾	SS2SEL ⁽²⁾	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	126
CCP1CON	P1M<	1:0> ⁽¹⁾	DC1B	<1:0>		CCP1M<3:0>			
CCP2CON	P2M<	1:0> ⁽¹⁾	DC2B	<1:0>		CCP2M<3:0>			
CCP3CON	_	-	DC3B	<1:0>		CCP3M<	:3:0>		240
CCP4CON	_	-	DC4B	<1:0>		CCP4M<3:0>			
CCPRxL	Capture/Com	pare/PWM Reg	gister x Low By	rte (LSB)					218*
CCPRxH	Capture/Com	pare/PWM Reg	gister x High B	yte (MSB)					218*
INLVLA	-	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLC	INLVLC7(2)	INLVLC6(2)	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	_	_	CCP2IE	95
PIE3	_	_	CCP4IE	CCP3IE	TMR6IE	_	TMR4IE	_	96
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	_	—	CCP2IF	99
PIR3	-	_	CCP4IF	CCP3IF	TMR6IF	_	TMR4IF	_	100
T1CON	TMR1C	S<1:0>	T1CKP	S<1:0>	T1OSCEN	T1SYNC	—	TMR10N	199
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/DONE	T1GVAL	T1GS	S<1:0>	200
TMR1L	Holding Regis	ster for the Lea	st Significant E	Byte of the 16-b	oit TMR1 Register				205*
TMR1H	Holding Regis	ster for the Mos	st Significant B	yte of the 16-b	it TMR1 Register				205*
TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISC	TRISC7 ⁽²⁾	TRISC6 ⁽²⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140

TABLE 24-4: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARE

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by Compare mode.

Note 1: Applies to ECCP modules only.

2: PIC16F/LF1829 only.

3: PIC16F/LF1825 only.

* Page provides register information.

24.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 24-3 shows a typical waveform of the PWM signal.

24.3.1 STANDARD PWM OPERATION

The standard PWM function described in this section is available and identical for CCP modules ECCP1, ECCP2, CCP3 and CCP4.

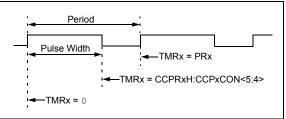
The standard PWM mode generates a Pulse-Width modulation (PWM) signal on the CCPx pin with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PRx registers
- TxCON registers
- · CCPRxL registers
- · CCPxCON registers

Figure 24-4 shows a simplified block diagram of PWM operation.

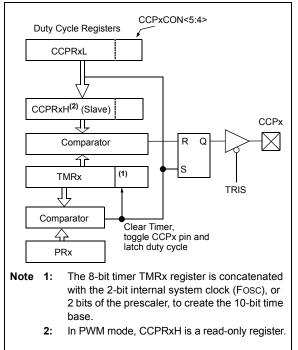
- Note 1: The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.
 - **2:** Clearing the CCPxCON register will relinquish control of the CCPx pin.

FIGURE 24-3: CCP PWM OUTPUT SIGNAL





SIMPLIFIED PWM BLOCK DIAGRAM



24.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

- 1. Disable the CCPx pin output driver by setting the associated TRIS bit.
- 2. Load the PRx register with the PWM period value.
- Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
- Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
- 5. Configure and start Timer2/4/6:
 - •Select the Timer2/4/6 resource to be used for PWM generation by setting the CxTSEL<1:0> bits in the CCPTMRS register.
 - •Clear the TMRxIF interrupt flag bit of the PIRx register. See Note below.
 - •Configure the TxCKPS bits of the TxCON register with the Timer prescale value.
 - •Enable the Timer by setting the TMRxON bit of the TxCON register.
- 6. Enable PWM output pin:
 - •Wait until the Timer overflows and the TMRxIF bit of the PIRx register is set. See Note below.
 - •Enable the CCPx pin output driver by clearing the associated TRIS bit.
- **Note:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

24.3.3 TIMER2/4/6 TIMER RESOURCE

The PWM standard mode makes use of one of the 8-bit Timer2/4/6 timer resources to specify the PWM period.

Configuring the CxTSEL<1:0> bits in the CCPTMRS register selects which Timer2/4/6 timer is used.

24.3.4 PWM PERIOD

The PWM period is specified by the PRx register of Timer2/4/6. The PWM period can be calculated using the formula of Equation 24-1.

EQUATION 24-1: PWM PERIOD

 $PWM Period = [(PRx) + 1] \bullet 4 \bullet TOSC \bullet$ (TMRx Prescale Value)

Note 1: Tosc = 1/Fosc

When TMRx is equal to PRx, the following three events occur on the next increment cycle:

- TMRx is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Note: The Timer postscaler (see Section 22.1 "Timer2/4/6 Operation") is not used in the determination of the PWM frequency.

24.3.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPRxL register and DCxB<1:0> bits of the CCPxCON register. The CCPRxL contains the eight MSbs and the DCxB<1:0> bits of the CCPxCON register contain the two LSbs. CCPRxL and DCxB<1:0> bits of the CCPxCON register can be written to at any time. The duty cycle value is not latched into CCPRxH until after the period completes (i.e., a match between PRx and TMRx registers occurs). While using the PWM, the CCPRxH register is read-only.

Equation 24-2 is used to calculate the PWM pulse width.

Equation 24-3 is used to calculate the PWM duty cycle ratio.

EQUATION 24-2: PULSE WIDTH

 $Pulse Width = (CCPRxL:CCPxCON < 5:4>) \bullet$

TOSC • (TMRx Prescale Value)

EQUATION 24-3: DUTY CYCLE RATIO

 $Duty Cycle Ratio = \frac{(CCPRxL:CCPxCON < 5:4>)}{4(PRx+1)}$

The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMRx register is concatenated with either the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2/4/6 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2bit latch, then the CCPx pin is cleared (see Figure 24-4).

24.3.6 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PRx is 255. The resolution is a function of the PRx register value as shown by Equation 24-4.

EQUATION 24-4: PWM RESOLUTION

Resolution =
$$\frac{\log[4(PRx+1)]}{\log(2)}$$
 bits

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 24-5:EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 32 MHz)

PWM Frequency	1.95 kHz	7.81 kHz	31.25 kHz	125 kHz	250 kHz	333.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 24-6: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 24-7: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

24.3.7 **OPERATION IN SLEEP MODE**

In Sleep mode, the TMRx register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMRx will continue from its previous state.

24.3.8 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See Section 5.0 "Oscillator Module (With Fail-Safe Clock Monitor)" for additional details.

24.3.9 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

ALTERNATE PIN LOCATIONS 24.3.10

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function registers, APFCON0 and APFCON1. To determine which pins can be moved and what their default locations are upon a Reset, see Section 12.1 "Alternate Pin Function" for more information.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page	
APFCON1	_	—	SDO2SEL ⁽²⁾	SS2SEL ⁽²⁾	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	126	
CCP1CON	P1M<	1:0> (1)	DC1B	<1:0>		CCP1I	240			
CCP2CON	P2M<	1:0> ⁽¹⁾	DC2B	<1:0>	:1:0> CCP2M<3:0>					
CCP3CON	—	—	DC3B<1:0>			CCP3I	240			
CCP4CON			DC4B	<1:0>		CCP4I	M<3:0>		240	
CCPTMRS	C4TSEL<1:0>		C3TSE	L<1:0>	C2TSE	L<1:0>	C1TSE	L<1:0>	241	
CCPR1L	Capture/Compare/PWM Register x Low Byte (LSB)					218*				
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131	
INLVLC	INLVLC7 ⁽²⁾	INLVLC6 ⁽²⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142	
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93	
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94	
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	_	_	CCP2IE	95	
PIE3	_	_	CCP4IE	CCP3IE	TMR6IE	—	TMR4IE	_	96	
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98	
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	_	CCP2IF	99	
PIR3	_	_	CCP4IF	CCP3IF	TMR6IF	—	TMR4IF	_	100	
PRx	Timer2/4/6 Pe	riod Register							203*	
T2CON	_		T2OUT	PS<3:0>		TMR2ON	T2CKP	'S<1:0>	205	
T4CON	_		T4OUTF	PS<3:0>		TMR4ON	T4CKP	'S<1:0>	205	
T6CON	_		T6OUT	PS<3:0>		TMR6ON	T6CKP	PS<1:0>	205	
TMRx	Timer2/4/6 Mo	dule Register							203*	
TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129	
TRISC	TRISC7 ⁽²⁾	TRISC6 ⁽²⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140	

TABLE 24-8: SUMMARY OF REGISTERS ASSOCIATED WITH STANDARD PWM

- = Unimplemented location, read as '0'. Shaded cells are not used by the PWM. Applies to ECCP modules only. Legend:

Note 1:

2: PIC16F/LF1829 only.

Page provides register information.

24.4 PWM (Enhanced Mode)

The enhanced PWM function described in this section is available for CCP modules ECCP1 and ECCP2, with any differences between modules noted.

The enhanced PWM mode generates a Pulse-Width Modulation (PWM) signal on up to four different output pins with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PRx registers
- TxCON registers
- · CCPRxL registers
- CCPxCON registers

The ECCP modules have the following additional PWM registers which control Auto-shutdown, Auto-restart, Dead-band Delay and PWM Steering modes:

- · CCPxAS registers
- PSTRxCON registers
- PWMxCON registers

The enhanced PWM module can generate the following five PWM Output modes:

- Single PWM
- Half-Bridge PWM
- Full-Bridge PWM, Forward Mode
- Full-Bridge PWM, Reverse Mode
- Single PWM with PWM Steering Mode

To select an Enhanced PWM Output mode, the PxM bits of the CCPxCON register must be configured appropriately.

The PWM outputs are multiplexed with I/O pins and are designated PxA, PxB, PxC and PxD. The polarity of the PWM pins is configurable and is selected by setting the CCPxM bits in the CCPxCON register appropriately.

Figure 24-5 shows an example of a simplified block diagram of the Enhanced PWM module.

Figure 24-8 shows the pin assignments for various Enhanced PWM modes.

- Note 1: The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.
 - 2: Clearing the CCPxCON register will relinquish control of the CCPx pin.
 - **3:** Any pin not used in the enhanced PWM mode is available for alternate pin functions, if applicable.
 - 4: To prevent the generation of an incomplete waveform when the PWM is first enabled, the ECCP module waits until the start of a new PWM period before generating a PWM signal.

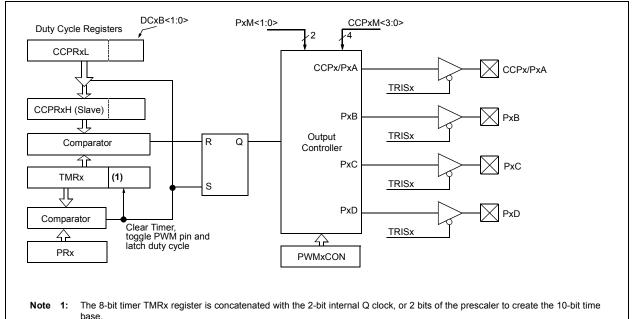


FIGURE 24-5: EXAMPLE SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODE

ECCP Mode	PxM<1:0>	CCPx/PxA	PxB	PxC	PxD
Single	00	Yes ⁽¹⁾	Yes ⁽¹⁾	Yes ⁽¹⁾	Yes ⁽¹⁾
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

TABLE 24-9: **EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES**

Note 1: PWM Steering enables outputs in Single mode.

EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH FIGURE 24-6: STATE)

PxM<1:0>	Signal	0 ◀ Pulse Width	PRX+1
		-	Period
00 (Single Output)	PxA Modulated		
	PxA Modulated	Delay ◀►►	Delay ▲►
10 (Half-Bridge)	PxB Modulated	_	
	PxA Active		
(Full-Bridge,	PxB Inactive		
⁰¹ Forward)	PxC Inactive	<u> </u>	
	PxD Modulated		
	PxA Inactive		
(Full-Bridge,	PxB Modulated		
Reverse)	PxC Active -		
	PxD Inactive -		

Period = 4 * Tosc * (PRx + 1) * (TMRx Prescale Value)
Pulse Width = Tosc * (CCPRxL<7:0>:CCPxCON<5:4>) * (TMRx Prescale Value)
Delay = 4 * Tosc * (PWMxCON<6:0>)

	FIGURE 24-7:	EXAMPLE ENHANCED PWM OUTPUT RELATIONSHIPS (ACTIVE-LOW STATE)
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:M<	1:0>	Signal	0	Pulse Width	→ Period →	
00	(Single Output)	PxA Modulated	= -			
		PxA Modulated		⊲ ⊳ Delay	→ Delay	į
10	(Half-Bridge)	PxB Modulated		Jelay		
		PxA Active			· · · · · · · · · · · · · · · · · · ·	
01	(Full-Bridge, Forward)	PxB Inactive	;		 	1 1 1
	i olwald)	PxC Inactive				
		PxD Modulated	į			
		PxA Inactive				
11	(Full-Bridge, Reverse)	PxB Modulated				i
	reverse)	PxC Active	— · — — ·		1 	
		PxD Inactive			 	

Pulse Width = Tosc * (CCPRxL<7:0>:CCPxCON<5:4>) * (TMRx Prescale Value)
Delay = 4 * Tosc * (PWMxCON<6:0>)

24.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCPx/PxA pin, while the complementary PWM output signal is output on the PxB pin (see Figure 24-9). This mode can be used for Half-Bridge applications, as shown in Figure 24-9, or for Full-Bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in Half-Bridge power devices. The value of the PDC<6:0> bits of the PWMxCON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See Section 24.4.5 "Programmable Dead-Band Delay Mode" for more details of the dead-band delay operations. Since the PxA and PxB outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure PxA and PxB as outputs.

FIGURE 24-8: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

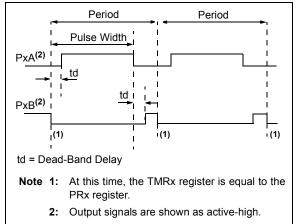
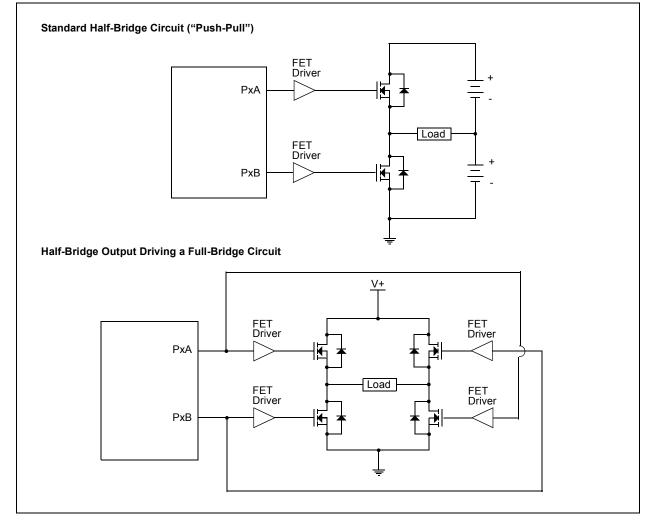


FIGURE 24-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS



24.4.2 FULL-BRIDGE MODE

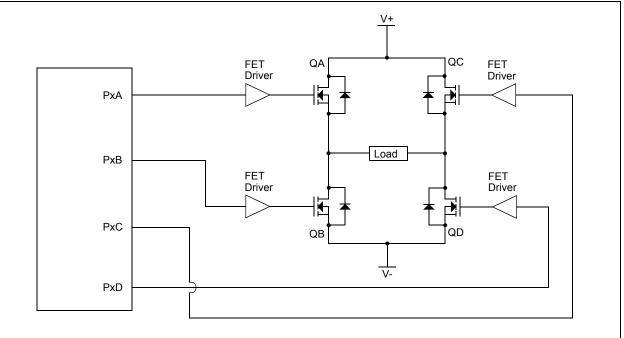
In Full-Bridge mode, all four pins are used as outputs. An example of Full-Bridge application is shown in Figure 24-10.

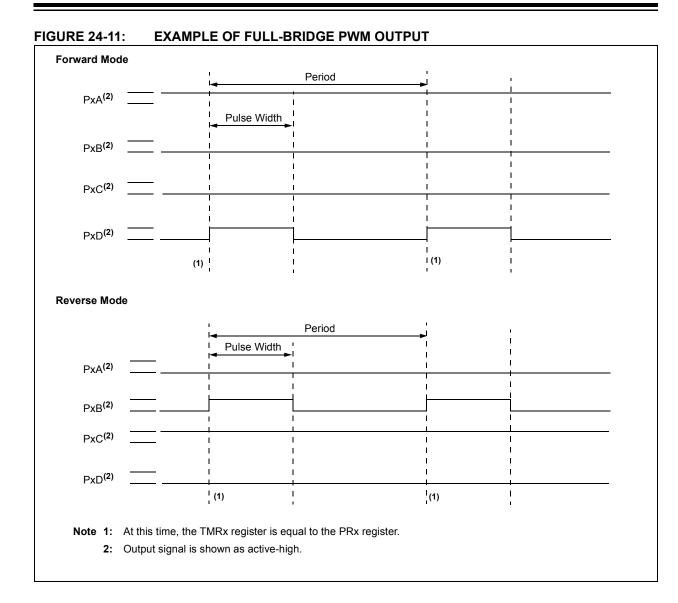
In the Forward mode, pin CCPx/PxA is driven to its active state, pin PxD is modulated, while PxB and PxC will be driven to their inactive state as shown in Figure 24-11.

In the Reverse mode, PxC is driven to its active state, pin PxB is modulated, while PxA and PxD will be driven to their inactive state as shown Figure 24-11.

PxA, PxB, PxC and PxD outputs are multiplexed with the PORT data latches. The associated TRIS bits must be cleared to configure the PxA, PxB, PxC and PxD pins as outputs.

FIGURE 24-10: EXAMPLE OF FULL-BRIDGE APPLICATION





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24.4.2.1 Direction Change in Full-Bridge Mode

In the Full-Bridge mode, the PxM1 bit in the CCPxCON register allows users to control the forward/reverse direction. When the application firmware changes this direction control bit, the module will change to the new direction on the next PWM cycle.

A direction change is initiated in software by changing the PxM1 bit of the CCPxCON register. The following sequence occurs four Timer cycles prior to the end of the current PWM period:

- The modulated outputs (PxB and PxD) are placed in their inactive state.
- The associated unmodulated outputs (PxA and PxC) are switched to drive in the opposite direction.
- PWM modulation resumes at the beginning of the next period.

See Figure 24-12 for an illustration of this sequence.

The Full-Bridge mode does not provide dead-band delay. As one output is modulated at a time, dead-band delay is generally not required. There is a situation where dead-band delay is required. This situation occurs when both of the following conditions are true:

- 1. The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
- 2. The turn-off time of the power switch, including the power device and driver circuit, is greater than the turn-on time.

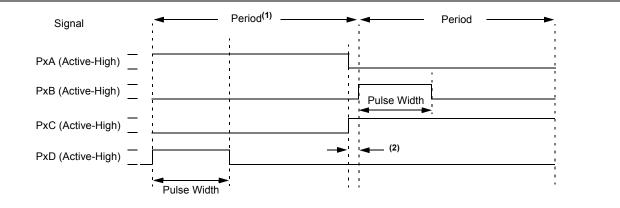
Figure 24-13 shows an example of the PWM direction changing from forward to reverse, at a near 100% duty cycle. In this example, at time t1, the output PxA and PxD become inactive, while output PxC becomes active. Since the turn-off time of the power devices is longer than the turn-on time, a shoot-through current will flow through power devices QC and QD (see Figure 24-10) for the duration of 't'. The same phenomenon will occur to power devices QA and QB for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for an application, two possible solutions for eliminating the shoot-through current are:

- 1. Reduce PWM duty cycle for one PWM period before changing directions.
- 2. Use switch drivers that can drive the switches off faster than they can drive them on.

Other options to prevent shoot-through current may exist.

FIGURE 24-12: EXAMPLE OF PWM DIRECTION CHANGE

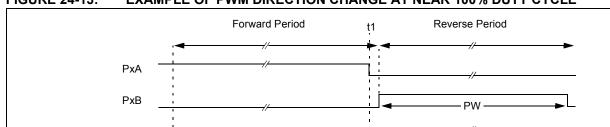


- **Note 1:** The direction bit PxM1 of the CCPxCON register is written any time during the PWM cycle.
 - 2: When changing directions, the PxA and PxC signals switch before the end of the current PWM cycle. The modulated PxB and PxD signals are inactive at this time. The length of this time is four Timer counts.

TON

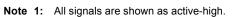
TOFF

T = TOFF - TON



ΡŴ

FIGURE 24-13: EXAMPLE OF PWM DIRECTION CHANGE AT NEAR 100% DUTY CYCLE



PxC

PxD

External Switch C

External Switch D

Shoot-Through Current

Potential

- 2: TON is the turn-on delay of power switch QC and its driver.
- 3: TOFF is the turn-off delay of power switch QD and its driver.

24.4.3 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the CCPxAS<2:0> bits of the CCPxAS register. A shutdown event may be generated by:

- A logic '0' on the INT pin
- A logic '1' on a Comparator (Cx) output

A shutdown condition is indicated by the CCPxASE (Auto-Shutdown Event Status) bit of the CCPxAS register. If the bit is a '0', the PWM pins are operating normally. If the bit is a '1', the PWM outputs are in the shutdown state.

When a shutdown event occurs, two things happen:

The CCPxASE bit is set to '1'. The CCPxASE will remain set until cleared in firmware or an auto-restart occurs (see Section 24.4.4 "Auto-Restart Mode").

The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs [PxA/PxC] and [PxB/PxD]. The state of each pin pair is determined by the PSSxAC and PSSxBD bits of the CCPxAS register. Each pin pair may be placed into one of three states:

- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

- Note 1: The auto-shutdown condition is a levelbased signal, not an edge-based signal. As long as the level is present, the autoshutdown will persist.
 - 2: Writing to the CCPxASE bit of the CCPxAS register is disabled while an auto-shutdown condition persists.
 - 3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart) the PWM signal will always restart at the beginning of the next PWM period.
 - 4: Prior to an auto-shutdown event caused by a comparator output or INT pin event, a software shutdown can be triggered in firmware by setting the CCPxASE bit of the CCPxAS register to '1'. The Auto-Restart feature tracks the active status of a shutdown caused by a comparator output or INT pin event only. If it is enabled at this time, it will immediately clear this bit and restart the ECCP module at the beginning of the next PWM period.

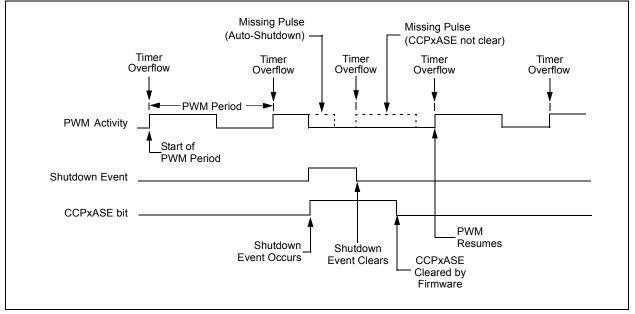
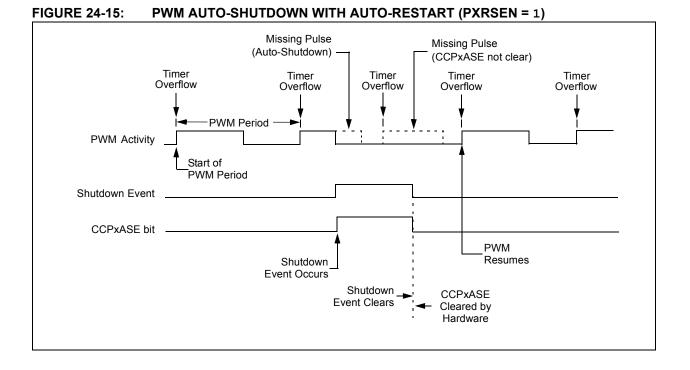


FIGURE 24-14: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PXRSEN = 0)

24.4.4 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PxRSEN bit in the PWMxCON register. If auto-restart is enabled, the CCPxASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the CCPxASE bit will be cleared via hardware and normal operation will resume.



24.4.5 PROGRAMMABLE DEAD-BAND DELAY MODE

In Half-Bridge applications where all power switches are modulated at the PWM frequency, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on, and the other turned off), both switches may be on for a short period of time until one switch completely turns off. During this brief interval, a very high current (*shoot-through current*) will flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In Half-Bridge mode, a digitally programmable deadband delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 24-16 for illustration. The lower seven bits of the associated PWMxCON register (Register 24-4) sets the delay period in terms of microcontroller instruction cycles (TcY or 4 Tosc).

FIGURE 24-16: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

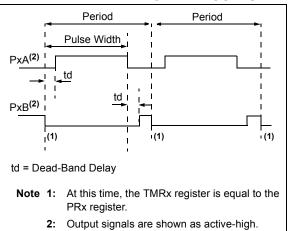
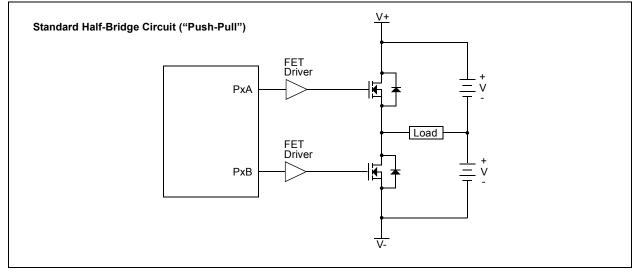


FIGURE 24-17: EXAMPLE OF HALF-BRIDGE APPLICATIONS



24.4.6 PWM STEERING MODE

In Single Output mode, PWM steering allows any of the PWM pins to be the modulated signal. Additionally, the same PWM signal can be simultaneously available on multiple pins.

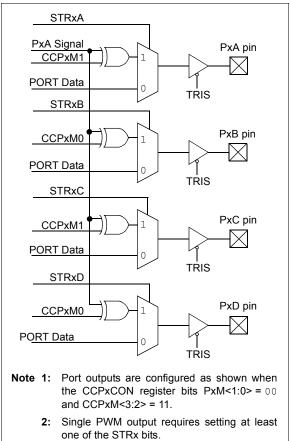
Once the Single Output mode is selected (CCPxM<3:2> = 11 and PxM<1:0> = 00 of the CCPxCON register), the user firmware can bring out the same PWM signal to one, two, three or four output pins by setting the appropriate STRx<D:A> bits of the PSTRxCON register, as shown in Table 24-8.

Note: The associated TRIS bits must be set to output ('0') to enable the pin output driver in order to see the PWM signal on the pin.

While the PWM Steering mode is active, CCPxM<1:0> bits of the CCPxCON register select the PWM output polarity for the Px<D:A> pins.

The PWM auto-shutdown operation also applies to PWM Steering mode as described in Section 24.4.3 "Enhanced PWM Auto-shutdown mode". An autoshutdown event will only affect pins that have PWM outputs enabled.

FIGURE 24-18: SIMPLIFIED STEERING BLOCK DIAGRAM



24.4.6.1 Steering Synchronization

The STRxSYNC bit of the PSTRxCON register gives the user two selections of when the steering event will happen. When the STRxSYNC bit is '0', the steering event will happen at the end of the instruction that writes to the PSTRxCON register. In this case, the output signal at the Px<D:A> pins may be an incomplete PWM waveform. This operation is useful when the user firmware needs to immediately remove a PWM signal from the pin.

When the STRxSYNC bit is '1', the effective steering update will happen at the beginning of the next PWM period. In this case, steering on/off the PWM output will always produce a complete PWM waveform.

Figures 24-19 and 24-20 illustrate the timing diagrams of the PWM steering depending on the STRxSYNC setting.

24.4.7 START-UP CONSIDERATIONS

When any PWM mode is used, the application hardware must use the proper external pull-up and/or pull-down resistors on the PWM output pins.

The CCPxM<1:0> bits of the CCPxCON register allow the user to choose whether the PWM output signals are active-high or active-low for each pair of PWM output pins (PxA/PxC and PxB/PxD). The PWM output polarities must be selected before the PWM pin output drivers are enabled. Changing the polarity configuration while the PWM pin output drivers are enable is not recommended since it may result in damage to the application circuits.

The PxA, PxB, PxC and PxD output latches may not be in the proper states when the PWM module is initialized. Enabling the PWM pin output drivers at the same time as the Enhanced PWM modes may cause damage to the application circuit. The Enhanced PWM modes must be enabled in the proper Output mode and complete a full PWM cycle before enabling the PWM pin output drivers. The completion of a full PWM cycle is indicated by the TMRxIF bit of the PIRx register being set as the second PWM period begins.

Note: When the microcontroller is released from Reset, all of the I/O pins are in the highimpedance state. The external circuits must keep the power switch devices in the Off state until the microcontroller drives the I/O pins with the proper signal levels or activates the PWM output(s).

24.4.8 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function registers, APFCON0 or APFCON1. To determine which pins can be moved and what their default locations are upon a Reset, see Section 12.1 "Alternate Pin Function" for more information.

FIGURE 24-19: EXAMPLE OF STEERING EVENT AT END OF INSTRUCTION (STRxSYNC = 0)

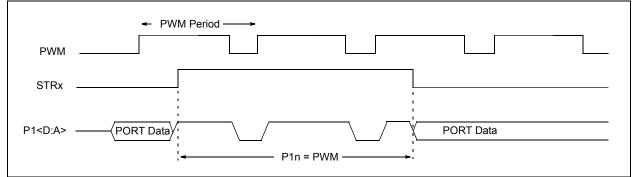
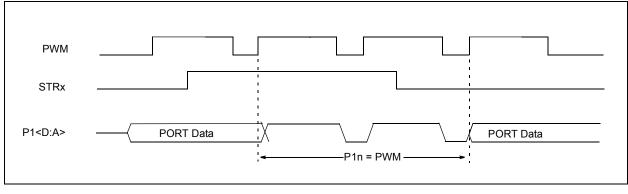


FIGURE 24-20: EXAMPLE OF STEERING EVENT AT BEGINNING OF INSTRUCTION (STRxSYNC = 1)



Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	—	—	SDO2SEL ⁽²⁾	SS2SEL ⁽²⁾	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	126
CCP1CON	P1M<	1:0> (1)	DC1B	<1:0>		CCP1I	M<3:0>		240
CCP2CON	P2M<	P2M<1:0> ⁽¹⁾ DC2B<1:0>			CCP2I	M<3:0>		240	
CCP3CON	-	_	- DC3B<1:0>			CCP3I	M<3:0>		240
CCP4CON	-	_	DC4B	<1:0>		CCP4I	M<3:0>		240
CCP1AS	CCP1ASE		CCP1AS<2:0>		PSS1A	\C<1:0>	PSS1B	D<1:0>	242
CCP2AS	CCP2ASE		CCP2AS<2:0>		PSS2A	\C<1:0>	PSS2B	D<1:0>	242
CCPTMRS	C4TSE	EL<1:0>	C3TSE	L<1:0>	C2TSE	EL<1:0>	C1TSE	L<1:0>	241
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	_	—	CCP2IE	95
PIE3	_	_	CCP4IE	CCP3IE	TMR6IE	—	TMR4IE	—	96
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	99
PIR3	_	—	CCP4IF	CCP3IF	TMR6IF	—	TMR4IF	—	100
PRx	Timer2/4/6 Pe	riod Register						-	213*
PSTR1CON	—	—	—	STR1SYNC	STR1D	STR1C	STR1B	STR1A	244
PSTR2CON	-	—	—	STR2SYNC	STR2D	STR2C	STR2B	STR2A	244
PWM1CON	P1RSEN				P1DC<6:0>				243
PWM2CON	P2RSEN				P2DC<6:0>				243
T2CON	-		T2OUT	PS<3:0>		TMR2ON	T2CKP	'S<1:0>	205
T4CON	_		T4OUTF	PS<3:0>		TMR4ON	T4CKP	'S<1:0>	205
T6CON	_		T6OUTF	PS<3:0>		TMR6ON	T6CKP	'S<1:0>	205
TMRx	Timer2/4/6 Mo	dule Register							203*
TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISC	TRISC7 ⁽²⁾	TRISC6 ⁽²⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140

TABLE 24-10: SUMMARY OF REGISTERS ASSOCIATED WITH ENHANCED PWM

 Legend:
 — = Unimplemented location, read as '0'. Shaded cells are not used by the PWM.

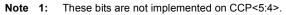
 Note
 1:
 Applies to ECCP modules only.

 2:
 PIC16F/LF1829 only.

 *
 Page provides register information.

REGISTER 24-1: CCPxCON: CCPx CONTROL REGISTER

R/W-00	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0				
PxN	//<1:0> ⁽¹⁾	DCxB	<1:0>		CCPx	V<3:0>					
bit 7							bit (
Legend:											
R = Readable	e bit	W = Writable bi	t	U = Unimpleme	ented bit, read as	; 'O'					
u = Bit is uncl	nanged	x = Bit is unkno	x = Bit is unknown -n/n = Value at POR and BOR/Value at all other								
'1' = Bit is set	e e	'0' = Bit is clear	ed								
bit 7-6	PxM<1:0>: Enhanced PWM Output Configuration bits ⁽¹⁾										
	<u>Capture mode</u> Unused	<u>>:</u>									
	<u>Compare mod</u> Unused	<u>Compare mode:</u> Unused									
	If CCPxM<3:2	<u>If CCPxM<3:2> = 00, 01, 10:</u>									
		xx = PxA assigned as Capture/Compare input; PxB, PxC, PxD assigned as port pins									
	01 = Full-Bridg 10 = Half-Bridg	I≥ = 11: utput; PxA modula ge output forward; ge output; PxA, Px ge output reverse;	PxD modulate B modulated w	ed; PxA active; PxI vith dead-band con	3, PxC inactive trol; PxC, PxD a	ssigned as port p	ins				
bit 5-4	DCxB<1:0>: PWM Duty Cycle Least Significant bits										
	Capture mode: Unused										
	Compare mode: Unused										
	PWM mode:										
	These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.										
bit 3-0	CCPxM<3:0>: ECCPx Mode Select bits										
	0000 = Capture/Compare/PWM off (resets ECCPx module)										
	0001 = Reserved										
	0010 = Compare mode: toggle output on match 0011 = Reserved										
		, vou									
	•	re mode: every fa	0 0								
		0101 = Capture mode: every rising edge									
	•	0110 = Capture mode: every 4th rising edge 0111 = Capture mode: every 16th rising edge									
	orre ouple	are model every h	stir noing eage								
		oare mode: initializ	•	· ·		,					
		pare mode: initializ									
	•	oare mode: genera			•		conversion if /				
	1011 = Compare mode: Special Event Trigger (ECCPx resets Timer, sets CCPxIF bit, starts A/D conversion if A D module is enabled) ⁽¹⁾										
	CCP Modules only:										
	11xx = PWM	mode									
	ECCP Module										
		I mode: PxA, PxC	-	-							
		I mode: PxA, PxC I mode: PxA, PxC	0,	,							
		I mode: PxA, PxC		-	1						
	1111 - 1 VVIV										



R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0		
C4TS	C4TSEL<1:0>		L<1:0>	C2TSE	L<1:0>	C1TSE	:L<1:0>		
bit 7							bit C		
Legend:									
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'			
u = Bit is unc	hanged	x = Bit is unkn	iown	-n/n = Value a	at POR and BC	R/Value at all	other Resets		
'1' = Bit is set	t	'0' = Bit is clea	ared						
bit 7-6	C4TSEL<1:0	>: CCP4 Timer	Selection bits	;					
	••••••	00 = CCP4 is based off Timer 2 in PWM Mode							
	01 = CCP4 is based off Timer 4 in PWM Mode								
	10 = CCP4 is based off Timer 6 in PWM Mode 11 = Reserved								
bit 5-4	C3TSEL<1:0>: CCP3 Timer Selection bits								
	00 = CCP3 is based off Timer 2 in PWM Mode								
		01 = CCP3 is based off Timer 4 in PWM Mode							
	10 = CCP3 is based off Timer 6 in PWM Mode								
	11 = Reserv	11 = Reserved							
bit 3-2	C2TSEL<1:0)>: CCP2 Timer	Selection bits	;					
		00 = CCP2 is based off Timer 2 in PWM Mode							
	01 = CCP2 is based off Timer 4 in PWM Mode								
	10 = CCP2 is based off Timer 6 in PWM Mode 11 = Reserved								
bit 1-0	C1TSEL<1:0	>: CCP1 Timer	Selection bits	i					
	00 = CCP1 i	00 = CCP1 is based off Timer 2 in PWM Mode							
	01 = CCP1 i	s based off Time	er 4 in PWM N	lode					
		s based off Time	er 6 in PWM N	lode					
	11 = Reserv	ed							

REGISTER 24-2: CCPTMRS: PWM TIMER SELECTION CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0						
CCPxASE	CPxASE CCPxAS<2:0>		•	PSSxA	C<1:0>	PSSxB	D<1:0>						
bit 7							bit (
Legend:													
R = Readable		W = Writable		•	nented bit, read								
u = Bit is uncl	•	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all	other Resets						
'1' = Bit is set		'0' = Bit is clea	ared										
bit 7			tdown Event (Yatua hit									
	CCPxASE: CCPx Auto-Shutdown Event Status bit												
	 1 = A shutdown event has occurred; CCPx outputs are in shutdown state 0 = CCPx outputs are operating 												
bit 6-4	CCxPAS<2:0>: CCPx Auto-Shutdown Source Select bits												
	000 = Auto-shutdown is disabled												
	001 = Comparator C1 output high ⁽¹⁾												
	010 = Comparator C2 output high ⁽¹⁾												
	011 = Either Comparator C1 or C2 high ⁽¹⁾ 100 = VIL on INT pin												
	101 = VIL on INT pin or Comparator C1 high ⁽¹⁾												
	110 = VIL on INT pin or Comparator C2 high ⁽¹⁾												
	111 = Vi∟ on INT pin or Comparator C1 or Comparator C2 high ⁽¹⁾												
bit 3-2	PSSxAC<1:0>: Pins PxA and PxC Shutdown State Control bits												
	00 = Drive pins PxA and PxC to '0'												
	01 = Drive pins PxA and PxC to '1'												
	1x = Pins PxA and PxC tri-state												
bit 1-0	PSSxBD<1:0>: Pins PxB and PxD Shutdown State Control bits												
				00 = Drive pins PxB and PxD to '0'									
	01 = Drive pins PxB and PxD to '1' 1x = Pins PxB and PxD tri-state												

REGISTER 24-3: CCPxAS: CCPx AUTO-SHUTDOWN CONTROL REGISTER

Note 1: If CxSYNC is enabled, the shutdown will be delayed by Timer1.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0				
PxRSEN				PxDC<6:0>							
bit 7			bit 0								
Legend:											
R = Readable bit W = Writable bit				U = Unimplemented bit, read as '0'							
u = Bit is unc	u = Bit is unchanged x = Bit is unknown				-n/n = Value at POR and BOR/Value at all other Resets						
'1' = Bit is set	t	'0' = Bit is cle	ared								
bit 7	PxRSEN: P	WM Restart Ena	able bit								
 1 = Upon auto-shutdown, the CCPxASE bit clears automatically once the shutdown event goes awa the PWM restarts automatically 0 = Upon auto-shutdown, CCPxASE must be cleared in software to restart the PWM 											
	-			st be cleared in s	soltware to resi	tart the Pyvivi					
bit 6-0	PxDC<6:0>	: PWM Delay Co	ount bits								
			. ,	cycles between e actual time it tr			a PWM signal				

REGISTER 24-4: PWMxCON: ENHANCED PWM CONTROL REGISTER

Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled.

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1				
_	—	_	STRxSYNC	STRxD	STRxC	STRxB	STRxA				
bit 7							bit 0				
Legend:											
R = Readal	ble bit	W = Writable	bit	U = Unimpler	mented bit, read	1 as '0'					
u = Bit is ur	nchanged	x = Bit is unk	nown	-n/n = Value a	at POR and BO	R/Value at all	other Resets				
'1' = Bit is s	set	'0' = Bit is cle	ared								
bit 7-5	Unimplemen	ted: Read as	'O'								
bit 4	STRxSYNC:	Steering Sync	bit								
	1 = Output st	1 = Output steering update occurs on next PWM period									
	0 = Output st	0 = Output steering update occurs at the beginning of the instruction cycle boundary									
bit 3	STRxD: Stee	STRxD: Steering Enable bit D									
	1 = PxD pin ł	nas the PWM v	vaveform with p	olarity control	from CCPxM<1	1:0>					
	0 = PxD pin i	0 = PxD pin is assigned to port pin									
bit 2	STRxC: Stee	STRxC: Steering Enable bit C									
	•	1 = PxC pin has the PWM waveform with polarity control from CCPxM<1:0>									
	0 = PxC pin i	s assigned to p	oort pin								
bit 1	STRxB: Stee	STRxB: Steering Enable bit B									
	1 = PxB pin h	1 = PxB pin has the PWM waveform with polarity control from CCPxM<1:0>									
	0 = PxB pin is	0 = PxB pin is assigned to port pin									
bit 0	STRxA: Stee	STRxA: Steering Enable bit A									
	1 = PxA pin h	nas the PWM w	vaveform with p	olarity control	from CCPxM<1	:0>					
	0 = PxA pin is	s assigned to p	oort pin								
Note 1 ·	The PWM Steerin	a mode is avai	lable only when		N register bits (~~PvM<3.2> -	- 11 and				

REGISTER 24-5: PSTRxCON: PWM STEERING CONTROL REGISTER⁽¹⁾

Note 1: The PWM Steering mode is available only when the CCPxCON register bits CCPxM<3:2> = 11 and PxM<1:0> = 00.

25.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP1 AND MSSP2) MODULE

25.1 Master SSPx (MSSPx) Module Overview

The Master Synchronous Serial Port (MSSPx) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSPx module can operate in one of two modes:

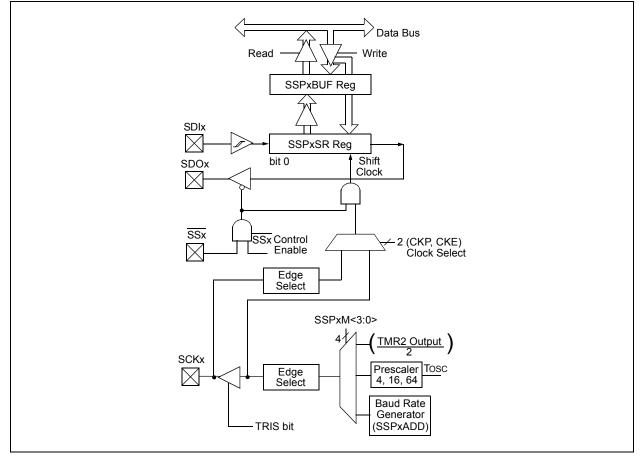
- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C[™])

The SPI interface supports the following modes and features:

- Master mode
- Slave mode
- · Clock Parity
- Slave Select Synchronization (Slave mode only)
- · Daisy chain connection of slave devices

Figure 25-1 is a block diagram of the SPI interface module.

FIGURE 25-1: MSSPX BLOCK DIAGRAM (SPI MODE)



PIC16F/LF1825/1829

The $\mathsf{I}^2\mathsf{C}$ interface supports the following modes and features:

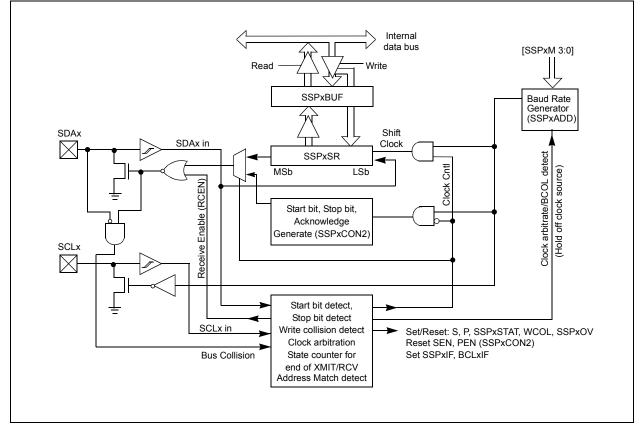
- Master mode
- Slave mode
- Byte NACKing (Slave mode)
- · Limited Multi-master support
- 7-bit and 10-bit addressing
- Start and Stop interrupts
- Interrupt masking
- Clock stretching
- · Bus collision detection
- · General call address matching
- Address masking
- · Address Hold and Data Hold modes
- · Selectable SDAx hold times

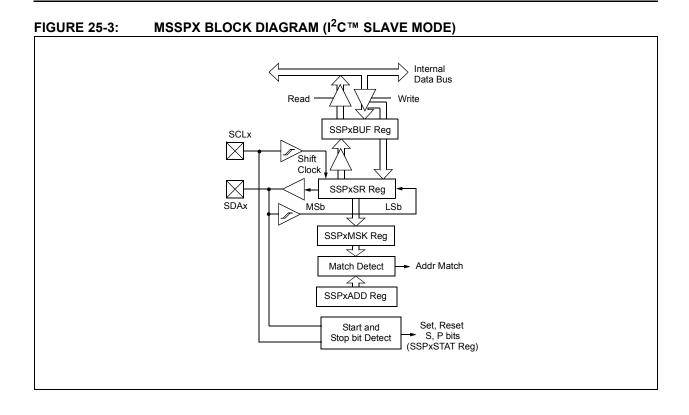
Figure 25-2 is a block diagram of the I^2C interface module in Master mode. Figure 25-3 is a diagram of the I^2C interface module in Slave mode.

The PIC16F1829 has two MSSP modules, MSSP1 and MSSP2, each module operating independently from the other.

- Note 1: In devices with more than one MSSP module, it is very important to pay close attention to SSPxCONx register names. SSP1CON1 and SSP1CON2 registers control different operational aspects of the same module, while SSP1CON1 and SSP2CON1 control the same features for two different modules.
 - 2: Throughout this section, generic references to an MSSP module in any of its operating modes may be interpreted as being equally applicable to MSSP1 or MSSP2. register names, module I/O signals, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module when required.

FIGURE 25-2: MSSPX BLOCK DIAGRAM (I²C[™] MASTER MODE)





25.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

- · Serial Clock (SCKx)
- Serial Data Out (SDOx)
- Serial Data In (SDIx)
- Slave Select (SSx)

Figure 25-1 shows the block diagram of the MSSPx module when operating in SPI Mode.

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

Figure 25-4 shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Transmissions involve two shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 25-5 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDOx output pin which is connected to, and received by, the slave's SDIx input pin. The slave device transmits information out on its SDOx output pin, which is connected to, and received by, the master's SDIx input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register. During each SPI clock cycle, a full duplex data transmission occurs. This means that while the master device is sending out the MSb from its shift register (on its SDOx pin) and the slave device is reading this bit and saving it as the LSb of its shift register, that the slave device is also sending out the MSb from its shift register (on its SDOx pin) and the master device is reading this bit and saving it as the LSb of its shift register.

After 8 bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

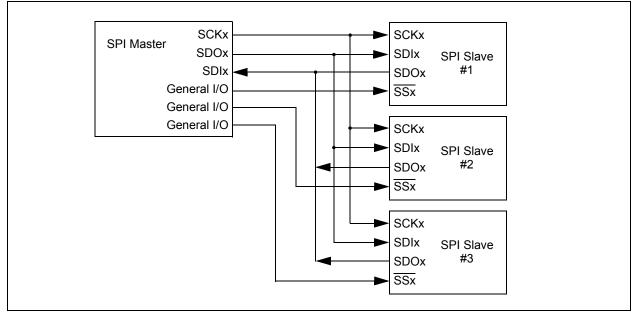
Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own.





25.2.1 SPI MODE REGISTERS

The MSSPx module has five registers for SPI mode operation. These are:

- MSSPx STATUS register (SSPxSTAT)
- MSSPx Control Register 1 (SSPxCON1)
- MSSPx Control Register 3 (SSPxCON3)
- MSSPx Data Buffer register (SSPxBUF)
- MSSPx Address register (SSPxADD)
- MSSPx Shift register (SSPxSR) (Not directly accessible)

SSPxCON1 and SSPxSTAT are the control and STATUS registers in SPI mode operation. The SSPxCON1 register is readable and writable. The lower 6 bits of the SSPxSTAT are read-only. The upper two bits of the SSPxSTAT are read/write.

In one SPI master mode, SSPxADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in Section 25.7 "Baud Rate Generator".

SSPxSR is the shift register used for shifting data in and out. SSPxBUF provides indirect access to the SSPxSR register. SSPxBUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSPxSR and SSPxBUF together create a buffered receiver. When SSPxSR receives a complete byte, it is transferred to SSPxBUF and the SSPxIF interrupt is set.

During transmission, the SSPxBUF is not buffered. A write to SSPxBUF will write to both SSPxBUF and SSPxSR.

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25.2.2 SPI MODE OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPxCON1<5:0> and SSPxSTAT<7:6>). These control bits allow the following to be specified:

- · Master mode (SCKx is the clock output)
- · Slave mode (SCKx is the clock input)
- Clock Polarity (Idle state of SCKx)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCKx)
- Clock Rate (Master mode only)
- · Slave Select mode (Slave mode only)

To enable the serial port, SSPx Enable bit, SSPxEN of the SSPxCON1 register, must be set. To reset or reconfigure SPI mode, clear the SSPxEN bit, re-initialize the SSPxCONx registers and then set the SSPxEN bit. This configures the SDIx, SDOx, SCKx and SSx pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- · SDIx must have corresponding TRIS bit set
- · SDOx must have corresponding TRIS bit cleared
- SCKx (Master mode) must have corresponding TRIS bit cleared
- SCKx (Slave mode) must have corresponding
 TRIS bit set
- SSx must have corresponding TRIS bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

The MSSPx consists of a transmit/receive shift register (SSPxSR) and a buffer register (SSPxBUF). The SSPxSR shifts the data in and out of the device, MSb first. The SSPxBUF holds the data that was written to the SSPxSR until the received data is ready. Once the 8 bits of data have been received, that byte is moved to the SSPxBUF register. Then, the Buffer Full Detect bit, BF of the SSPxSTAT register, and the interrupt flag bit, SSPxIF, are set. This double-buffering of the received data (SSPxBUF) allows the next byte to start reception before reading the data that was just received. Any write to the **SSPxBUF** reaister durina transmission/reception of data will be ignored and the write collision detect bit WCOL of the SSPxCON1 register, will be set. User software must clear the WCOL bit to allow the following write(s) to the SSPxBUF register to complete successfully.

When the application software is expecting to receive valid data, the SSPxBUF should be read before the next byte of data to transfer is written to the SSPxBUF. The Buffer Full bit, BF of the SSPxSTAT register, indicates when SSPxBUF has been loaded with the received data (transmission is complete). When the SSPxBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSPx interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur.

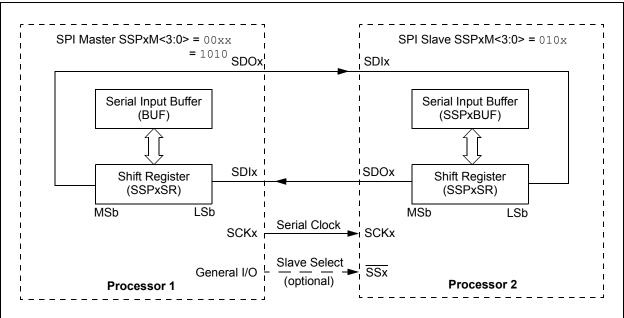


FIGURE 25-5: SPI MASTER/SLAVE CONNECTION

25.2.3 SPI MASTER MODE

The master can initiate the data transfer at any time because it controls the SCKx line. The master determines when the slave (Processor 2, Figure 25-5) is to broadcast data by the software protocol.

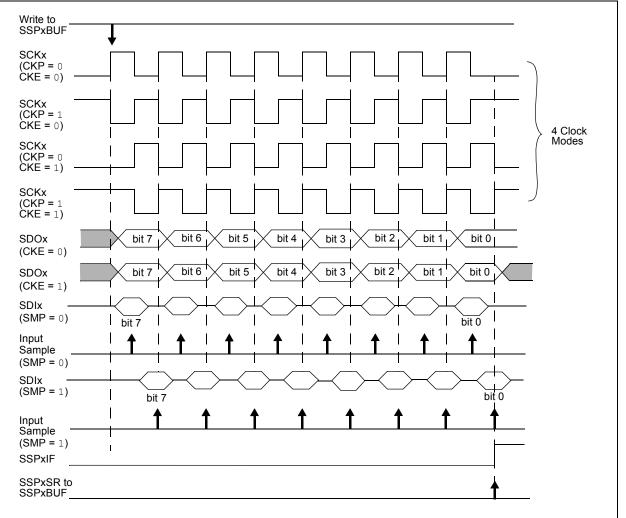
In Master mode, the data is transmitted/received as soon as the SSPxBUF register is written to. If the SPI is only going to receive, the SDOx output could be disabled (programmed as an input). The SSPxSR register will continue to shift in the signal present on the SDIx pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPxBUF register as if a normal received byte (interrupts and Status bits appropriately set). The clock polarity is selected by appropriately programming the CKP bit of the SSPxCON1 register and the CKE bit of the SSPxSTAT register. This then, would give waveforms for SPI communication as shown in Figure 25-6, Figure 25-8 and Figure 25-9, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 * Tcy)
- Fosc/64 (or 16 * Tcy)
- · Timer2 output/2
- Fosc/(4 * (SSPxADD + 1))

Figure 25-6 shows the waveforms for Master mode.

When the CKE bit is set, the SDOx data is valid before there is a clock edge on SCKx. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPxBUF is loaded with the received data is shown.

FIGURE 25-6: SPI MODE WAVEFORM (MASTER MODE)



25.2.4 SPI SLAVE MODE

In Slave mode, the data is transmitted and received as external clock pulses appear on SCKx. When the last bit is latched, the SSPxIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCKx pin. The Idle state is determined by the CKP bit of the SSPxCON1 register.

While in Slave mode, the external clock is supplied by the external clock source on the SCKx pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCKx pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

25.2.4.1 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device.

Figure 25-7 shows the block diagram of a typical Daisy-Chain connection when operating in SPI Mode.

In a daisy-chain configuration, only the most recent byte on the bus is required by the slave. Setting the BOEN bit of the SSPxCON3 register will enable writes to the SSPxBUF register, even if the previous byte has not been read. This allows the software to ignore data that may not apply to it.

25.2.5 SLAVE SELECT SYNCHRONIZATION

The Slave Select can also be used to synchronize communication. The Slave Select line is held high until the master device is ready to communicate. When the Slave Select line is pulled low, the slave knows that a new transmission is starting.

If the slave fails to receive the communication properly, it will be reset at the end of the transmission, when the Slave Select line returns to a high state. The slave is then ready to receive a new transmission when the Slave Select line is pulled low again. If the Slave Select line is not used, there is a risk that the slave will eventually become out of sync with the master. If the slave misses a bit, it will always be one bit off in future transmissions. Use of the Slave Select line allows the slave and master to align themselves at the beginning of each transmission.

The \overline{SSx} pin allows a Synchronous Slave mode. The SPI must be in Slave mode with \overline{SSx} pin control enabled (SSPxCON1<3:0> = 0100).

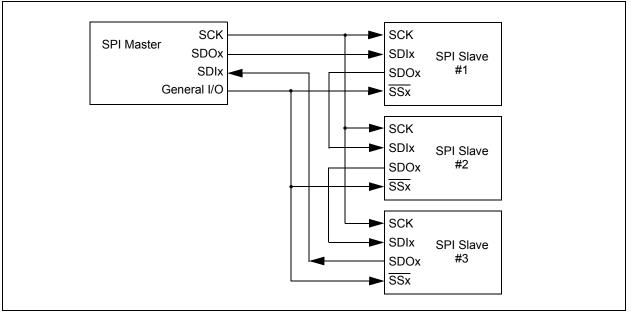
When the \overline{SSx} pin is low, transmission and reception are enabled and the SDOx pin is driven.

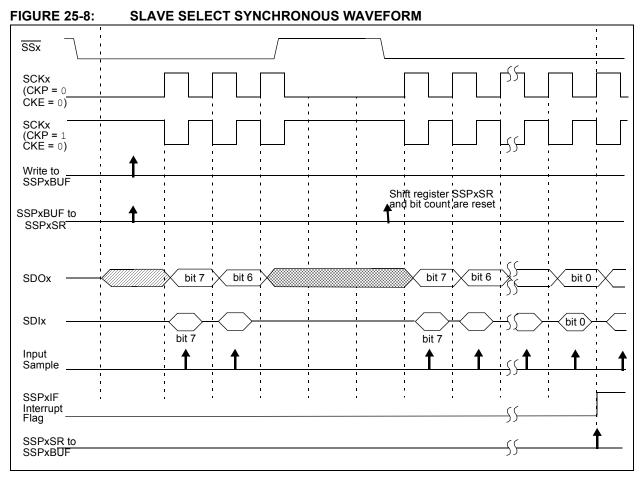
When the \overline{SSx} pin goes high, the SDOx pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

Note 1:	When the SPI is in Slave mode with \overline{SSx} pin control enabled (SSPxCON1<3:0> = 0100), the SPI module will reset if the \overline{SSx} pin is set to VDD.
2:	When the SPI is used in Slave mode with CKE set; the user must enable SSx pin control.
3:	While operated in SPI Slave mode the SMP bit of the SSPxSTAT register must remain clear.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the SSx pin to a high level or clearing the SSPxEN bit.





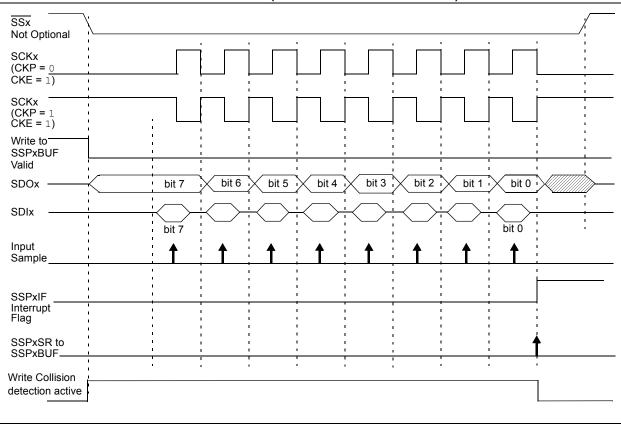


PIC16F/LF1825/1829

1100ILE 20 0.	0111							•)		
SSx Optional										
SCKx (CKP = <u>0</u> CKE = 0)	1 1 1 1									
SCKx (CKP = 1 CKE = 0)	1 1 1 1									<u> </u>
Write to SSPxBUF Valid	1 1 1 1	 		 		I I I I	 	1 1 1 1	 	
SDOx —	-{[]]]]]]]]]]]]]]]]]]]]]]]]]]]]]]]]]]]]	📈 bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	· · · · ·
SDIx ———		bit 7	\sim	\sim		\sim			bit 0	
Input	I I	. ▲		. ▲	. ▲		▲	▲	. ▲	
Sample	1 1			<u>ı </u>	<u>ı </u>		<u>ı </u>	1 	<u> </u>	
SSPxIF Interrupt Flag	1 1 1 1 1			 	 		 	 		
SSPxSR to	i I	1 1	I I	1 1	1	I I	1 1	1	♠	
SSPxBUF	+								• • • •	
Write Collision detection active										

FIGURE 25-9: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

FIGURE 25-10: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



25.2.6 SPLOPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in full power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSPx clock is much faster than the system clock.

In Slave mode, when MSSPx interrupts are enabled, after the master completes sending data, an MSSPx interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSPx interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all 8 bits have been received, the MSSPx interrupt flag bit will be set and if enabled, will wake the device.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	_	_	ANSA4	—	ANSA2	ANSA1	ANSA0	129
ANSELB ⁽¹⁾	ANSB7	ANSB6	ANSB5	ANSB4	_	_	_	_	136
ANSELC	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	_	-	ANSC3	ANSC2	ANSC1	ANSC0	141
APFCON0	RXDTSEL	SDOSEL ⁽²⁾	SSSEL ⁽²⁾	_	T1GSEL	TXCKSEL	_	—	125
APFCON1	—		SDO2SEL ⁽¹⁾	SS2SEL ⁽¹⁾	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	126
INLVLA	_		INLVLA5 ⁽¹⁾	INLVLA4 ⁽¹⁾	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	_	-	_	-	136
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1 ⁽¹⁾	INLVLC0 ⁽¹⁾	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
SSP1BUF	SSP1BUF Synchronous Serial Port Receive Buffer/Transmit Register							249*	
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>			294	
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	296
SSP1STAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	293
TRISA	—	—	TRISA5 ⁽¹⁾	TRISA4 ⁽¹⁾	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	_	_	—	_	135
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1 ⁽¹⁾	TRISC0 ⁽¹⁾	140

TABLE 25-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the MSSP1 in SPI mode.

Page provides register information. Note

1: PIC16F/LF1829 only.

2: PIC16F/LF1825 only.

25.3 I²C MODE OVERVIEW

The Inter-Integrated Circuit Bus (I²C) is a multi-master serial data communication bus. Devices communicate in a master/slave environment where the master devices initiate the communication. A Slave device is controlled through addressing.

The I²C bus specifies two signal connections:

- · Serial Clock (SCLx)
- Serial Data (SDAx)

Figure 25-11 shows the block diagram of the MSSPx module when operating in I^2C mode.

Both the SCLx and SDAx connections are bidirectional open-drain lines, each requiring pull-up resistors for the supply voltage. Pulling the line to ground is considered a logical zero and letting the line float is considered a logical one.

Figure 25-11 shows a typical connection between two processors configured as master and slave devices.

The I^2C bus can operate with one or more master devices and one or more slave devices.

There are four potential modes of operation for a given device:

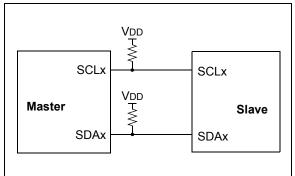
- Master Transmit mode
 (master is transmitting data to a slave)
- Master Receive mode
 (master is receiving data from a slave)
- Slave Transmit mode (slave is transmitting data to a master)
- Slave Receive mode (slave is receiving data from the master)

To begin communication, a master device starts out in Master Transmit mode. The master device sends out a Start bit followed by the address byte of the slave it intends to communicate with. This is followed by a single Read/Write bit, which determines whether the master intends to transmit to or receive data from the slave device.

If the requested slave exists on the bus, it will respond with an Acknowledge bit, otherwise known as an ACK. The master then continues in either Transmit mode or Receive mode and the slave continues in the complement, either in Receive mode or Transmit mode, respectively.

A Start bit is indicated by a high-to-low transition of the SDAx line while the SCLx line is held high. Address and data bytes are sent out, Most Significant bit (MSb) first. The Read/Write bit is sent out as a logical one when the master intends to read data from the slave, and is sent out as a logical zero when it intends to write data to the slave.

FIGURE 25-11: I²C MASTER/ SLAVE CONNECTION



The Acknowledge bit (\overline{ACK}) is an active-low signal, which holds the SDAx line low to indicate to the transmitter that the slave device has received the transmitted data and is ready to receive more.

The transition of a data bit is always performed while the SCLx line is held low. Transitions that occur while the SCLx line is held high are used to indicate Start and Stop bits.

If the master intends to write to the slave, then it repeatedly sends out a byte of data, with the slave responding after each byte with an \overrightarrow{ACK} bit. In this example, the master device is in Master Transmit mode and the slave is in Slave Receive mode.

If the master intends to read from the slave, then it repeatedly receives a byte of data from the slave, and responds after each byte with an \overline{ACK} bit. In this example, the master device is in Master Receive mode and the slave is Slave Transmit mode.

On the last byte of data communicated, the master device may end the transmission by sending a Stop bit. If the master device is in Receive mode, it sends the Stop bit in place of the last ACK bit. A Stop bit is indicated by a low-to-high transition of the SDAx line while the SCLx line is held high.

In some cases, the master may want to maintain control of the bus and re-initiate another transmission. If so, the master device may send another Start bit in place of the Stop bit or last ACK bit when it is in receive mode.

The I²C bus specifies three message protocols;

- Single message where a master writes data to a slave.
- Single message where a master reads data from a slave.
- Combined message where a master initiates a minimum of two writes, or two reads, or a combination of writes and reads, to one or more slaves.

When one device is transmitting a logical one, or letting the line float, and a second device is transmitting a logical zero, or holding the line low, the first device can detect that the line is not a logical one. This detection, when used on the SCLx line, is called clock stretching. Clock stretching gives slave devices a mechanism to control the flow of data. When this detection is used on the SDAx line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

25.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of Clock Stretching. An addressed slave device may hold the SCLx clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCLx line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCLx connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

25.3.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDAx data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels don't match, loses arbitration, and must stop transmitting on the SDAx line.

For example, if one transmitter holds the SDAx line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDAx line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDAx line. If this transmitter is also a master device, it also must stop driving the SCLx line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDAx line continues with its original transmission. It can do so without any complications, because so far, the transmission appears exactly as expected with no other transmitter disturbing the message.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

If two master devices are sending a message to two different slave devices at the address stage, the master sending the lower slave address always wins arbitration. When two master devices send messages to the same slave address, and addresses can sometimes refer to multiple slaves, the arbitration process must continue into the data stage.

Arbitration usually occurs very rarely, but it is a necessary process for proper multi-master support.

25.4 I²C MODE OPERATION

All MSSPx I²C communication is byte oriented and shifted out MSb first. Six SFR registers and 2 interrupt flags interface the module with the PIC[®] microcontroller and user software. Two pins, SDAx and SCLx, are exercised by the module to communicate with other external I²C devices.

25.4.1 BYTE FORMAT

All communication in I^2C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the 8th falling edge of the SCLx line, the device outputting data on the SDAx changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCLx, is provided by the master. Data is valid to change while the SCLx signal is low, and sampled on the rising edge of the clock. Changes on the SDAx line while the SCLx line is high define special conditions on the bus, explained below.

25.4.2 DEFINITION OF I²C TERMINOLOGY

There is language and terminology in the description of I^2C communication that have definitions specific to I^2C . That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Phillips I^2C specification.

25.4.3 SDAX AND SCLX PINS

Selection of any I²C mode with the SSPxEN bit set, forces the SCLx and SDAx pins to be open-drain. These pins should be set by the user to inputs by setting the appropriate TRIS bits.

Note:	Data	is	tied	to	output	zero	when	an	I ² C
	mode is enabled.								

25.4.4 SDAX HOLD TIME

The hold time of the SDAx pin is selected by the SDAHT bit of the SSPxCON3 register. Hold time is the time SDAx is held valid after the falling edge of SCLx. Setting the SDAHT bit selects a longer 300 ns minimum hold time and may help on buses with large capacitance.

TABLE 25-2:I²C BUS TERMS

TADLE 23-2.	
TERM	Description
Transmitter	The device which shifts data out onto the bus.
Receiver	The device which shifts data in from the bus.
Master	The device that initiates a transfer, generates clock signals and termi- nates a transfer.
Slave	The device addressed by the mas- ter.
Multi-master	A bus with more than one device that can initiate data transfers.
Arbitration	Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted.
Synchronization	Procedure to synchronize the clocks of two or more devices on the bus.
Idle	No master is controlling the bus, and both SDAx and SCLx lines are high.
Active	Any time one or more master devices are controlling the bus.
Addressed Slave	Slave device that has received a matching address and is actively being clocked by a master.
Matching Address	Address byte that is clocked into a slave that matches the value stored in SSPxADD.
Write Request	Slave receives a matching address with R/W bit clear, and is ready to clock in data.
Read Request	Master sends an address byte with the R/W bit set, indicating that it wishes to clock data out of the Slave. This data is the next and all following bytes until a Restart or Stop.
Clock Stretching	When a device on the bus hold SCLx low to stall communication.
Bus Collision	Any time the SDAx line is sampled low by the module while it is out- putting and expected high state.

25.4.5 START CONDITION

The I^2C specification defines a Start condition as a transition of SDAx from a high to a low state while SCLx line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 25-10 shows wave forms for Start and Stop conditions.

A bus collision can occur on a Start condition if the module samples the SDAx line low before asserting it low. This does not conform to the I²C Specification that states no bus collision can occur on a Start.

25.4.6 STOP CONDITION

A Stop condition is a transition of the SDAx line from low-to-high state while the SCLx line is high.

Note: At least one SCLx low time must appear before a Stop is valid, therefore, if the SDAx line goes low then high again while the SCLx line stays high, only the Start condition is detected.

25.4.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave.

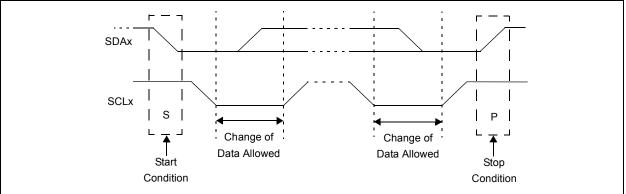
In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/\overline{W} bit set. The slave logic will then hold the clock and prepare to clock out data.

After a full match with R/\overline{W} clear in 10-bit mode, a prior match flag is set and maintained. Until a Stop condition, a high address with R/\overline{W} clear, or high address match fails.

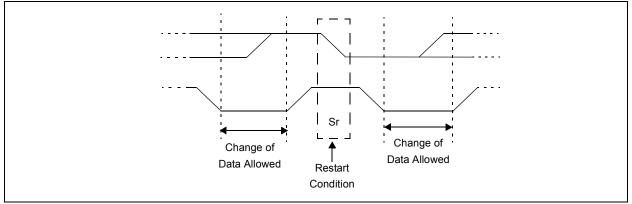
25.4.8 START/STOP CONDITION INTERRUPT MASKING

The SCIE and PCIE bits of the SSPxCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. Slave modes where interrupt on Start and Stop detect are already enabled, these bits will have no effect.









25.4.9 ACKNOWLEDGE SEQUENCE

The 9th SCLx pulse for any transferred byte in I^2C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDAx line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge (ACK) is an active-low signal, pulling the SDAx line low indicated to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an \overline{ACK} is placed in the ACKSTAT bit of the SSPxCON2 register.

Slave software, when the AHEN and DHEN bits are set, allow the user to set the ACK value sent back to the transmitter. The ACKDT bit of the SSPxCON2 register is set/cleared to determine the response.

Slave hardware will generate an ACK response if the AHEN and DHEN bits of the SSPxCON3 register are clear.

There are certain conditions where an ACK will not be sent by the slave. If the BF bit of the SSPxSTAT register or the SSPxOV bit of the SSPxCON1 register are set when a byte is received.

When the module is addressed, after the 8th falling edge of SCLx on the bus, the ACKTIM bit of the SSPxCON3 register is set. The ACKTIM bit indicates the acknowledge time of the active bus. The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is enabled.

25.5 I²C SLAVE MODE OPERATION

The MSSPx Slave mode operates in one of four modes selected in the SSPxM bits of SSPxCON1 register. The modes can be divided into 7-bit and 10-bit Addressing mode. 10-bit Addressing modes operate the same as 7-bit with some additional overhead for handling the larger addresses.

Modes with Start and Stop bit interrupts operated the same as the other modes with SSPxIF additionally getting set upon detection of a Start, Restart or Stop condition.

25.5.1 SLAVE MODE ADDRESSES

The SSPxADD register (Register 25-6) contains the Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPxBUF register and an interrupt is generated. If the value does not match, the module goes Idle and no indication is given to the software that anything happened.

The SSPx Mask register (Register 25-5) affects the address matching process. See **Section 25.5.9 "SSPx Mask Register"** for more information.

25.5.1.1 I²C Slave 7-bit Addressing Mode

In 7-bit Addressing mode, the LSb of the received data byte is ignored when determining if there is an address match.

25.5.1.2 I²C Slave 10-bit Addressing Mode

In 10-bit Addressing mode, the first received byte is compared to the binary value of '1 1 1 1 0 A9 A8 0'. A9 and A8 are the two MSb of the 10-bit address and stored in bits 2 and 1 of the SSPxADD register.

After the acknowledge of the high byte the UA bit is set and SCLx is held low until the user updates SSPxADD with the low address. The low address byte is clocked in and all 8 bits are compared to the low address value in SSPxADD. Even if there is not an address match; SSPxIF and UA are set, and SCLx is held low until SSPxADD is updated to receive a high byte again. When SSPxADD is updated the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-bit addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/W bit set. The slave hardware will then acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address byte match.

25.5.2 SLAVE RECEPTION

When the R/\overline{W} bit of a matching received address byte is clear, the R/\overline{W} bit of the SSPxSTAT register is cleared. The received address is loaded into the SSPxBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF bit of the SSPxSTAT register is set, or bit SSPxOV bit of the SSPxCON1 register is set. The BOEN bit of the SSPxCON3 register modifies this operation. For more information see Register 25-4.

An MSSPx interrupt is generated for each transferred data byte. Flag bit, SSPxIF, must be cleared by software.

When the SEN bit of the SSPxCON2 register is set, SCLx will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPxCON1 register, except sometimes in 10-bit mode. See Section 25.2.3 "SPI Master Mode" for more detail.

25.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSPx module configured as an I^2C Slave in 7-bit Addressing mode. All decisions made by hardware or software and their effect on reception. Figure 25-13 and Figure 25-14 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I^2C communication.

- 1. Start bit detected.
- 2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- 3. Matching address with R/\overline{W} bit clear is received.
- 4. The slave pulls SDAx low sending an ACK to the master, and sets SSPxIF bit.
- 5. Software clears the SSPxIF bit.
- 6. Software reads received address from SSPxBUF clearing the BF flag.
- 7. If SEN = 1; Slave software sets CKP bit to release the SCLx line.
- 8. The master clocks out a data byte.
- 9. Slave drives SDAx low sending an ACK to the master, and sets SSPxIF bit.
- 10. Software clears SSPxIF.
- 11. Software reads the received byte from SSPxBUF clearing BF.
- 12. Steps 8-12 are repeated for all received bytes from the Master.
- 13. Master sends Stop condition, setting P bit of SSPxSTAT, and the bus goes Idle.

25.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the 8th falling edge of SCLx. These additional interrupts allow the slave software to decide whether it wants to ACK the receive address or data byte, rather than the hardware. This functionality adds support for PMBus[™] that was not present on previous versions of this module.

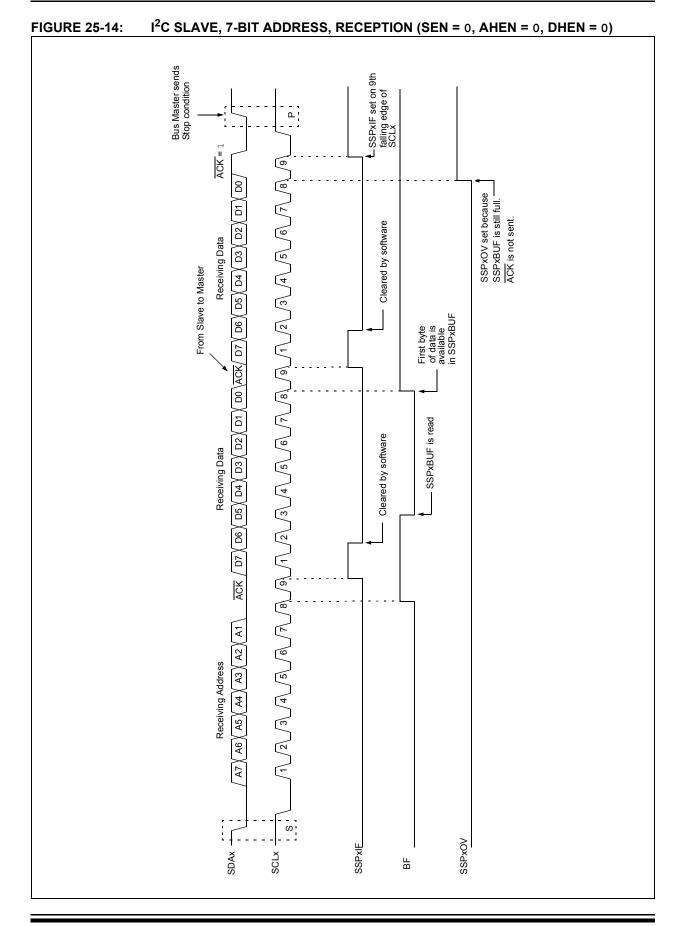
This list describes the steps that need to be taken by slave software to use these options for $I^{2}C$ communcation. Figure 25-15 displays a module using both address and data holding. Figure 25-16 includes the operation with the SEN bit of the SSPxCON2 register set.

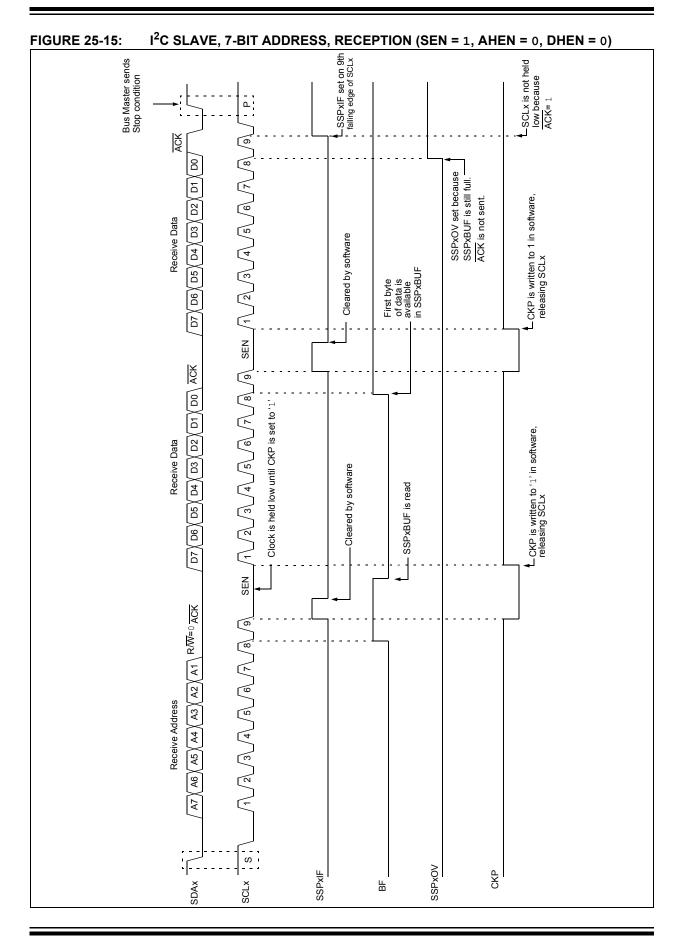
- 1. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- Matching address with R/W bit clear is clocked in. SSPxIF is set and CKP cleared after the 8th falling edge of SCLx.
- 3. Slave clears the SSPxIF.
- Slave can look at the ACKTIM bit of the SSPxCON3 register to <u>determine</u> if the SSPxIF was after or before the ACK.
- 5. Slave reads the address value from SSPxBUF, clearing the BF flag.
- 6. Slave sets ACK value clocked out to the master by setting ACKDT.
- 7. Slave releases the clock by setting CKP.
- 8. SSPxIF is set after an ACK, not after a NACK.
- 9. If SEN = 1 the slave hardware will stretch the clock after the ACK.

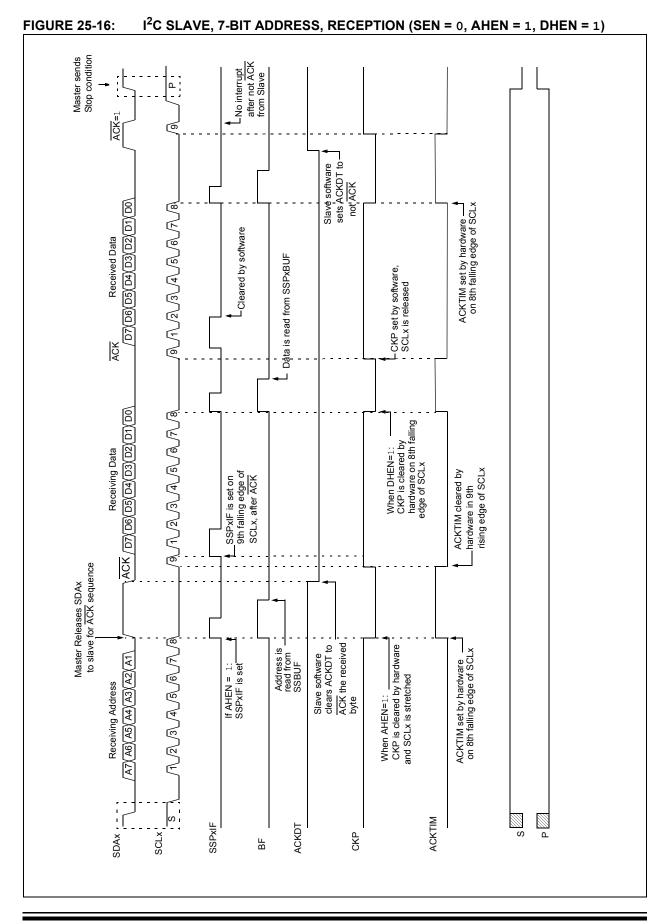
10. Slave clears SSPxIF.

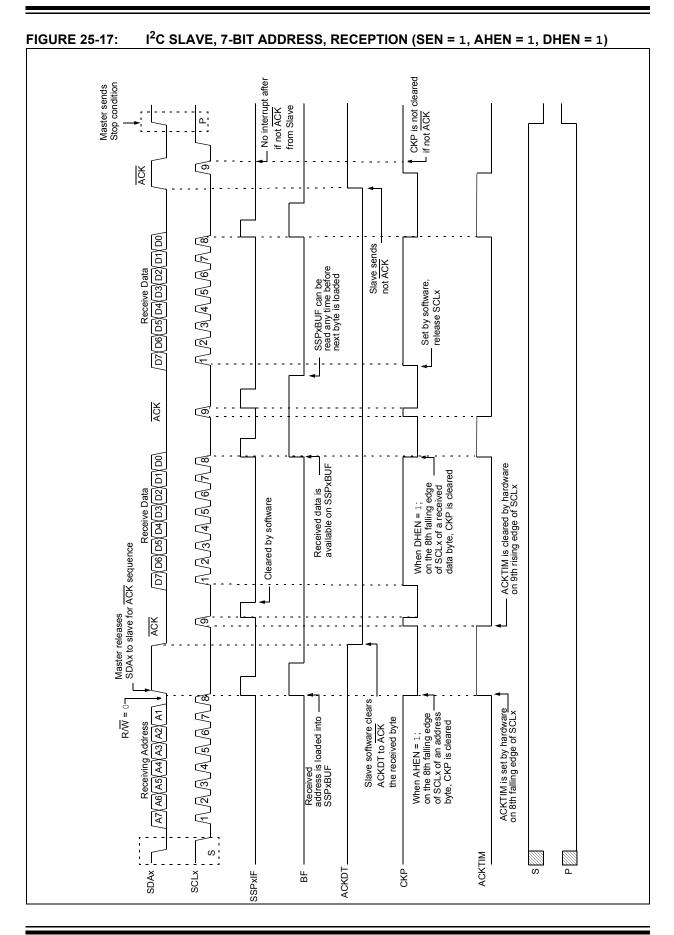
Note: SSPxIF is still set after the 9th falling edge of SCLx even if there is no clock stretching and BF has been cleared. Only if NACK is sent to Master is SSPxIF not set

- 11. SSPxIF set and CKP cleared after 8th falling edge of SCLx for a received data byte.
- 12. Slave looks at ACKTIM bit of SSPxCON3 to determine the source of the interrupt.
- 13. Slave reads the received data from SSPxBUF clearing BF.
- 14. Steps 7-14 are the same for each received data byte.
- 15. Communication is ended by either the slave sending an ACK = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSTSTAT register.









25.5.3 SLAVE TRANSMISSION

When the R/\overline{W} bit of the incoming address byte is set and an address match occurs, the R/\overline{W} bit of the SSPxSTAT register is set. The received address is loaded into the SSPxBUF register, and an ACK pulse is sent by the slave on the ninth bit.

Following the ACK, slave hardware clears the CKP bit and the SCLx pin is held low (see Section 25.5.6 "Clock Stretching" for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data.

The transmit data must be loaded into the SSPxBUF register which also loads the SSPxSR register. Then the SCLx pin should be released by setting the CKP bit of the SSPxCON1 register. The eight data bits are shifted out on the falling edge of the SCLx input. This ensures that the SDAx signal is valid during the SCLx high time.

The ACK pulse from the master-receiver is latched on the rising edge of the ninth SCLx input pulse. This ACK value is copied to the ACKSTAT bit of the SSPxCON2 register. If ACKSTAT is set (not ACK), then the data transfer is complete. In this case, when the not ACK is latched by the slave, the slave goes Idle and waits for another occurrence of the Start bit. If the SDAx line was low (ACK), the next transmit data must be loaded into the SSPxBUF register. Again, the SCLx pin must be released by setting bit CKP.

An MSSPx interrupt is generated for each data transfer byte. The SSPxIF bit must be cleared by software and the SSPxSTAT register is used to determine the status of the byte. The SSPxIF bit is set on the falling edge of the ninth clock pulse.

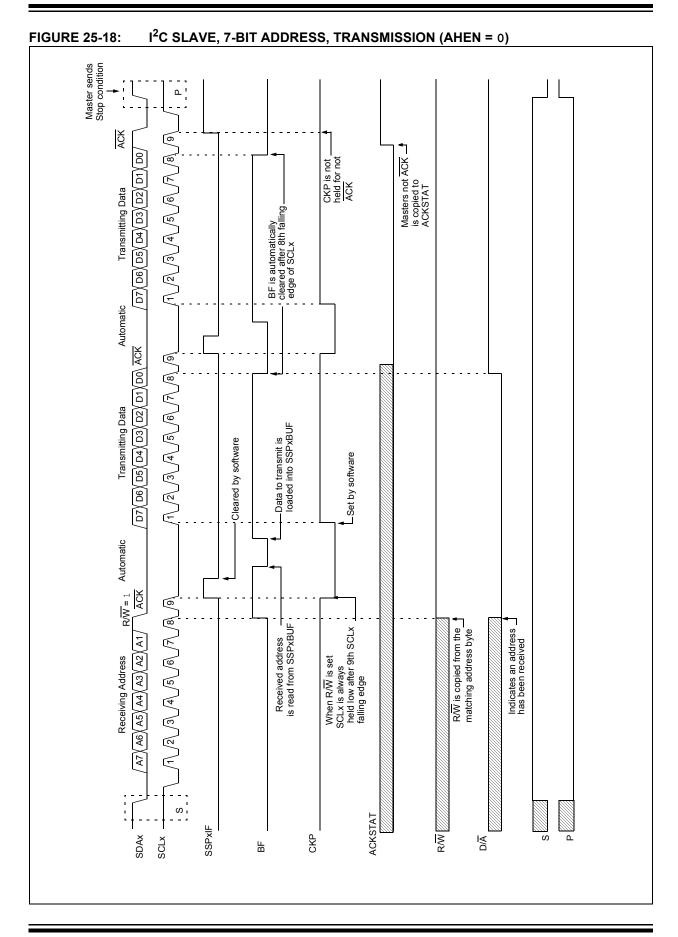
25.5.3.1 Slave Mode Bus Collision

A slave receives a Read request and begins shifting data out on the SDAx line. If a bus collision is detected and the SBCDE bit of the SSPxCON3 register is set, the BCLxIF bit of the PIRx register is set. Once a bus collision is detected, the slave goes Idle and waits to be addressed again. User software can use the BCLxIF bit to handle a slave bus collision.

25.5.3.2 7-bit Transmission

A master device can transmit a read request to a slave, and then clock data out of the slave. The list below outlines what software for a slave will need to do to accomplish a standard transmission. Figure 25-17 can be used as a reference to this list.

- 1. Master sends a Start condition on SDAx and SCLx.
- 2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- Matching address with R/W bit set is received by the Slave setting SSPxIF bit.
- 4. Slave hardware generates an ACK and sets SSPxIF.
- 5. SSPxIF bit is cleared by user.
- 6. Software reads the received address from SSPxBUF, clearing BF.
- 7. R/\overline{W} is set so CKP was automatically cleared after the ACK.
- 8. The slave software loads the transmit data into SSPxBUF.
- 9. CKP bit is set releasing SCLx, allowing the master to clock the data out of the slave.
- 10. SSPxIF is set after the ACK response from the master is loaded into the ACKSTAT register.
- 11. SSPxIF bit is cleared.
- 12. The slave software checks the ACKSTAT bit to see if the master wants to clock out more data.
 - **Note 1:** If the master ACKs the clock will be stretched.
 - ACKSTAT is the only bit updated on the rising edge of SCLx (9th) rather than the falling.
- 13. Steps 9-13 are repeated for each transmitted byte.
- 14. If the master sends a not ACK; the clock is not held, but SSPxIF is still set.
- 15. The master sends a Restart condition or a Stop.
- 16. The slave is no longer addressed.



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25.5.3.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit of the SSPxCON3 register enables additional clock stretching and interrupt generation after the 8th falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSPxIF interrupt is set.

Figure 25-18 displays a standard waveform of a 7-bit Address Slave Transmission with AHEN enabled.

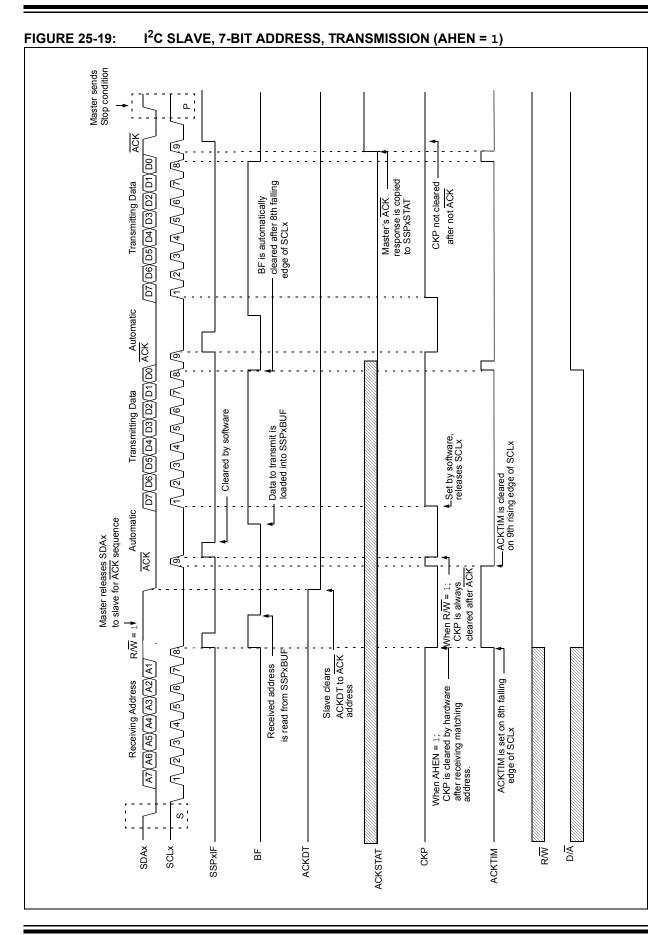
- 1. Bus starts Idle.
- Master sends Start condition; the S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- Master sends matching address with R/W bit set. After the 8th falling edge of the SCLx line the CKP bit is cleared and SSPxIF interrupt is generated.
- 4. Slave software clears SSPxIF.
- 5. Slave software reads ACKTIM bit of SSPxCON3 register, and R/W and D/A of the SSPxSTAT register to determine the source of the interrupt.
- 6. Slave reads the address value from the SSPxBUF register clearing the BF bit.
- 7. Slave software decides from this information if it wishes to ACK or not ACK and sets the ACKDT bit of the SSPxCON2 register accordingly.
- 8. Slave sets the CKP bit releasing SCLx.
- 9. Master clocks in the \overline{ACK} value from the slave.
- 10. Slave hardware automatically clears the CKP bit and sets SSPxIF after the ACK if the R/W bit is set.
- 11. Slave software clears SSPxIF.
- 12. Slave loads value to transmit to the master into SSPxBUF setting the BF bit.

Note: <u>SSPxBUF</u> cannot be loaded until after the <u>ACK</u>.

13. Slave sets CKP bit releasing the clock.

- 14. Master clocks out the data from the slave and sends an ACK value on the 9th SCLx pulse.
- 15. Slave hardware copies the ACK value into the ACKSTAT bit of the SSPxCON2 register.
- 16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
- 17. If the master sends a not \overline{ACK} the slave releases the bus allowing the master to send a Stop and end the communication.

Note: Master must send a not ACK on the last byte to ensure that the slave releases the SCLx line to receive a Stop.



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25.5.4 SLAVE MODE 10-BIT ADDRESS RECEPTION

This section describes a standard sequence of events for the MSSPx module configured as an I^2C Slave in 10-bit Addressing mode.

Figure 25-19 is used as a visual reference for this description.

This is a step by step process of what must be done by slave software to accomplish I^2C communication.

- 1. Bus starts Idle.
- Master sends Start condition; S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- Master sends matching high address with the R/W bit clear; UA bit of the SSPxSTAT register is set.
- 4. Slave sends ACK and SSPxIF is set.
- 5. Software clears the SSPxIF bit.
- 6. Software reads received address from SSPxBUF clearing the BF flag.
- 7. Slave loads low address into SSPxADD, releasing SCLx.
- 8. Master sends matching low address byte to the slave; UA bit is set.

Note: Updates to the SSPxADD register are not allowed until after the ACK sequence.

9. Slave sends ACK and SSPxIF is set.

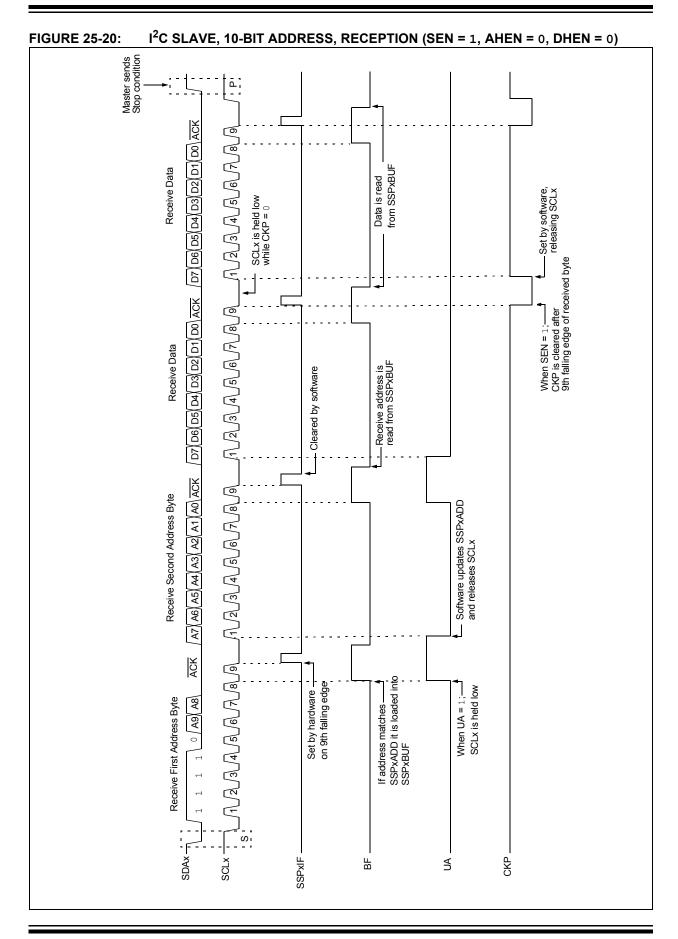
Note: If the low address does not match, SSPxIF and UA are still set so that the slave software can set SSPxADD back to the high address. BF is not set because there is no match. CKP is unaffected.

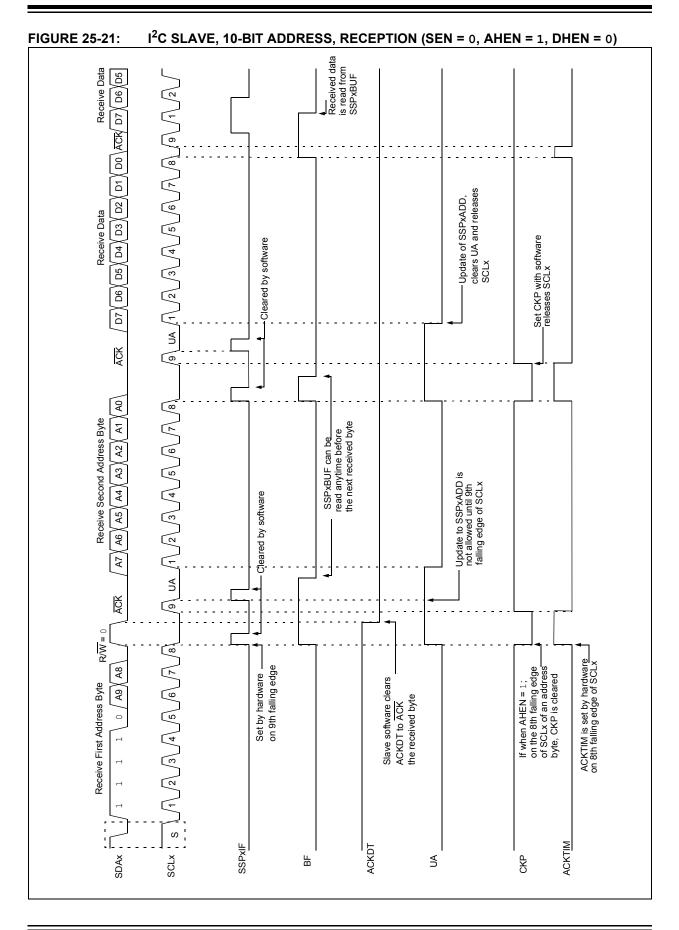
- 10. Slave clears SSPxIF.
- 11. Slave reads the received matching address from SSPxBUF clearing BF.
- 12. Slave loads high address into SSPxADD.
- 13. Master clocks a data <u>byte</u> to the slave and clocks out the slaves ACK on the 9th SCLx pulse; SSPxIF is set.
- 14. If SEN bit of SSPxCON2 is set, CKP is cleared by hardware and the clock is stretched.
- 15. Slave clears SSPxIF.
- 16. Slave reads the received byte from SSPxBUF clearing BF.
- 17. If SEN is set the slave sets CKP to release the SCLx.
- 18. Steps 13-17 repeat for each received byte.
- 19. Master sends Stop to end the transmission.

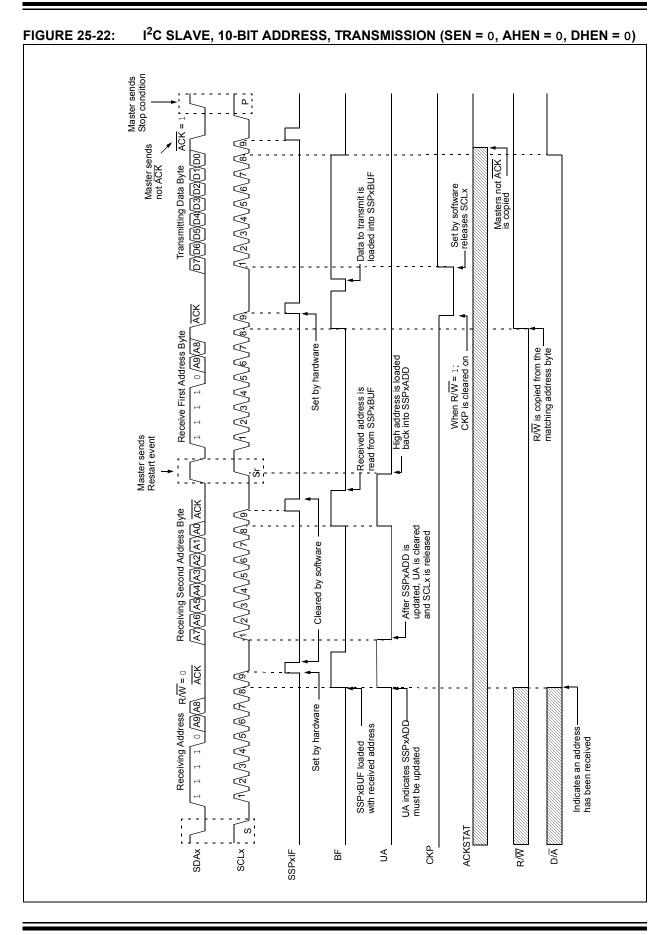
25.5.5 10-BIT ADDRESSING WITH ADDRESS OR DATA HOLD

Reception using 10-bit addressing with AHEN or DHEN set is the same as with 7-bit modes. The only difference is the need to update the SSPxADD register using the UA bit. All functionality, specifically when the CKP bit is cleared and SCLx line is held low are the same. Figure 25-20 can be used as a reference of a slave in 10-bit addressing with AHEN set.

Figure 25-21 shows a standard waveform for a slave transmitter in 10-bit Addressing mode.







25.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCLx line low effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCLx.

The CKP bit of the SSPxCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCLx line to go low and then hold it. Setting CKP will release SCLx and allow more communication.

25.5.6.1 Normal Clock Stretching

Following an ACK if the R/W bit of SSPxSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPxBUF with data to transfer to the master. If the SEN bit of SSPxCON2 is set, the slave hardware will always stretch the clock after the ACK sequence. Once the slave is ready; CKP is set by software and communication resumes.

- **Note 1:** The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPxBUF was read before the 9th falling edge of SCLx.
 - 2: Previous versions of the module did not stretch the clock for a transmission if SSPxBUF was loaded before the 9th falling edge of SCLx. It is now always cleared for read requests.

25.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set, the clock is always stretched. This is the only time the SCLx is stretched without CKP being cleared. SCLx is released immediately after a write to SSPxADD.

Note:	Previous versions of the module did not
	stretch the clock if the second address byte
	did not match.

25.5.6.3 Byte NACKing

When AHEN bit of SSPxCON3 is set; CKP is cleared by hardware after the 8th falling edge of SCLx for a received matching address byte. When DHEN bit of SSPxCON3 is set; CKP is cleared after the 8th falling edge of SCLx for received data.

Stretching after the 8th falling edge of SCLx allows the slave to look at the received address or data and decide if it wants to ACK the received data.

25.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCLx line to go low and then hold it. However, clearing the CKP bit will not assert the SCLx output low until the SCLx output is already sampled low. Therefore, the CKP bit will not assert the SCLx line until an external I^2C master device has already asserted the SCLx line. The SCLx output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCLx. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCLx (see Figure 25-22).

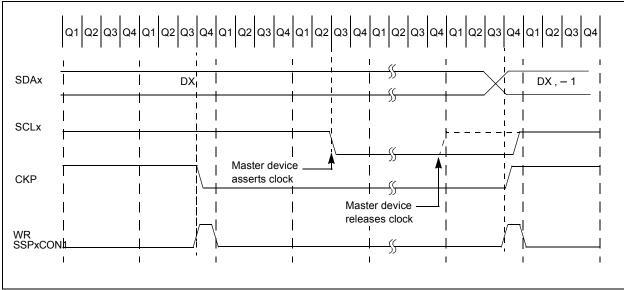


FIGURE 25-23: CLOCK SYNCHRONIZATION TIMING

25.5.8 GENERAL CALL ADDRESS SUPPORT

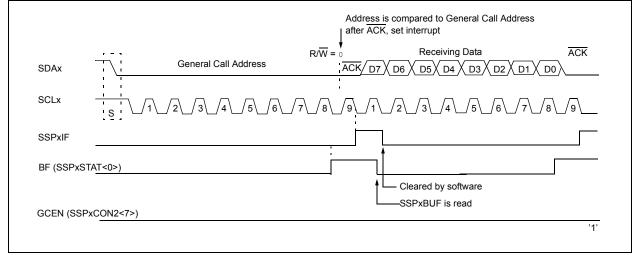
The addressing procedure for the I^2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the I^2C protocol, defined as address 0x00. When the GCEN bit of the SSPxCON2 register is set, the slave module will automatically ACK the reception of this address regardless of the value stored in SSPxADD. After the slave clocks in an address of all zeros with the R/W bit clear, an interrupt is generated and slave software can read SSPxBUF and respond. Figure 25-23 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPxCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the 8th falling edge of SCLx. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.





25.5.9 SSPX MASK REGISTER

An SSPx Mask (SSPxMSK) register (Register 25-5) is available in I²C Slave mode as a mask for the value held in the SSPxSR register during an address comparison operation. A zero ('0') bit in the SSPxMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSPx operation until written with a mask value.

The SSPx Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSPx mask has no effect during the reception of the first (high) byte of the address.

25.6 I²C MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPxM bits in the SSPxCON1 register and by setting the SSPxEN bit. In Master mode, the SCLx and SDAx lines are set as inputs and are manipulated by the MSSPx hardware.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSPx module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is Idle.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit condition detection. Start and Stop condition detection is the only active circuitry in this mode. All other communication is done by the user software directly manipulating the SDAx and SCLx lines.

The following events will cause the SSPx Interrupt Flag bit, SSPxIF, to be set (SSPx interrupt, if enabled):

- · Start condition detected
- · Stop condition detected
- · Data transfer byte transmitted/received
- Acknowledge transmitted/received
- · Repeated Start generated
- Note 1: The MSSPx module, when configured in I²C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPxBUF register to initiate transmission before the Start condition is complete. In this case, the SSPxBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPxBUF did not occur
 - 2: When in Master mode, Start/Stop detection is masked and an interrupt is generated when the SEN/PEN bit is cleared and the generation is complete.

25.6.1 I²C MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDAx, while SCLx outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic '0'. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

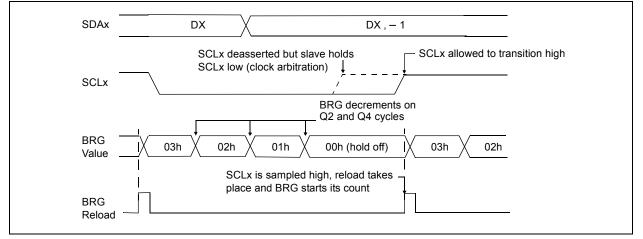
In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate the receive bit. Serial data is received via SDAx, while SCLx outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

A Baud Rate Generator is used to set the clock frequency output on SCLx. See **Section 25.7 "Baud Rate Generator"** for more detail.

25.6.2 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCLx pin (SCLx allowed to float high). When the SCLx pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCLx pin is actually sampled high. When the SCLx pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and begins counting. This ensures that the SCLx high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 25-25).

FIGURE 25-25: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



25.6.3 WCOL STATUS FLAG

If the user writes the SSPxBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPxBUF was attempted while the module was not Idle.

Note:	Because queueing of events is not
	allowed, writing to the lower 5 bits of
	SSPxCON2 is disabled until the Start
	condition is complete.

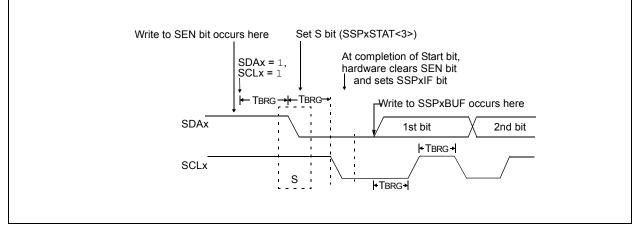
25.6.4 I²C MASTER MODE START CONDITION TIMING

To initiate a Start condition, the user sets the Start Enable bit, SEN bit of the SSPxCON2 register. If the SDAx and SCLx pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and starts its count. If SCLx and SDAx are both sampled high when the Baud Rate Generator times out (TBRG), the SDAx pin is driven low. The action of the SDAx being driven low while SCLx is high is the Start condition and causes the S bit of the SSPxSTAT1 register to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit of the SSPxCON2 register will be automatically cleared

FIGURE 25-26: FIRST START BIT TIMING

by hardware; the Baud Rate Generator is suspended, leaving the SDAx line held low and the Start condition is complete.

- Note 1: If at the beginning of the Start condition, the SDAx and SCLx pins are already sampled low, or if during the Start condition, the SCLx line is sampled low before the SDAx line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLxIF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.
 - **2:** The Philips I²C Specification states that a bus collision cannot occur on a Start.

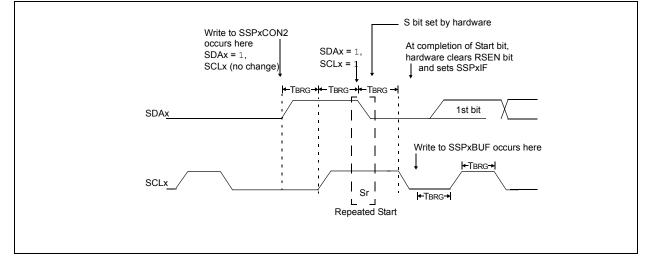


25.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit of the SSPxCON2 register is programmed high and the Master state machine is no longer active. When the RSEN bit is set, the SCLx pin is asserted low. When the SCLx pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDAx pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDAx is sampled high, the SCLx pin will be deasserted (brought high). When SCLx is sampled high, the Baud Rate Generator is reloaded and begins counting. SDAx and SCLx must be sampled high for one TBRG. This action is then followed by assertion of the SDAx pin (SDAx = 0) for one TBRG while SCLx is high. SCLx is asserted low. Following this, the RSEN bit of the SSPxCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDAx pin held low. As soon as a Start condition is detected on the SDAx and SCLx pins, the S bit of the SSPxSTAT register will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

- Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.
 - **2:** A bus collision during the Repeated Start condition occurs if:
 - SDAx is sampled low when SCLx goes from low-to-high.
 - SCLx goes low before SDAx is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 25-27: REPEAT START CONDITION WAVEFORM



25.6.6 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPxBUF register. This action will set the Buffer Full flag bit, BF and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDAx pin after the falling edge of SCLx is asserted. SCLx is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCLx is released high. When the SCLx pin is released high, it is held that way for TBRG. The data on the SDAx pin must remain stable for that duration and some hold time after the next falling edge of SCLx. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDAx. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time if an address match occurred, or if data was received properly. The status of ACK is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPxIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPxBUF, leaving SCLx low and SDAx unchanged (Figure 25-27).

After the write to the SSPxBUF, each bit of the address will be shifted out on the falling edge of SCLx until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will release the SDAx pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDAx pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT Status bit of the SSPxCON2 register. Following the falling edge of the ninth clock transmission of the address, the SSPxIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPxBUF takes place, holding SCLx low and allowing SDAx to float.

25.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSPxSTAT register is set when the CPU writes to SSPxBUF and is cleared when all 8 bits are shifted out.

25.6.6.2 WCOL Status Flag

If the user writes the SSPxBUF when a transmit is already in progress (i.e., SSPxSR is still shifting out a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

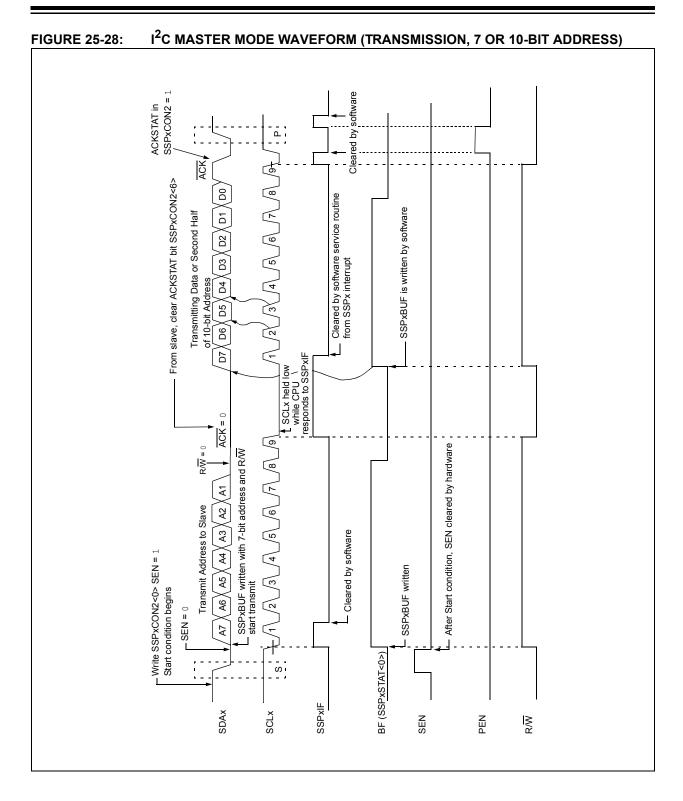
WCOL must be cleared by software before the next transmission.

25.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSPxCON2 register is cleared when the slave has sent an Acknowledge ($\overrightarrow{ACK} = 0$) and is set when the slave does not Acknowledge ($\overrightarrow{ACK} = 1$). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

25.6.6.4 Typical transmit sequence:

- 1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
- 2. SSPxIF is set by hardware on completion of the Start.
- 3. SSPxIF is cleared by software.
- 4. The MSSPx module will wait the required start time before any other operation takes place.
- 5. The user loads the SSPxBUF with the slave address to transmit.
- Address is shifted out the SDAx pin until all 8 bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
- The MSSPx module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
- The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
- 9. The user loads the SSPxBUF with eight bits of data.
- 10. Data is shifted out the SDAx pin until all 8 bits are transmitted.
- 11. The MSSPx module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
- 12. Steps 8-11 are repeated for all transmitted data bytes.
- 13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSPxCON2 register. Interrupt is generated once the Stop/Restart condition is complete.



25.6.7 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN bit of the SSPxCON2 register.

Note:	The MSSPx module must be in an Idle
	state before the RCEN bit is set or the
	RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCLx pin changes (high-to-low/low-to-high) and data is shifted into the SSPxSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPxSR are loaded into the SSPxBUF, the BF flag bit is set, the SSPxIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCLx low. The MSSPx is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPxCON2 register.

25.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPxBUF from SSPxSR. It is cleared when the SSPxBUF register is read.

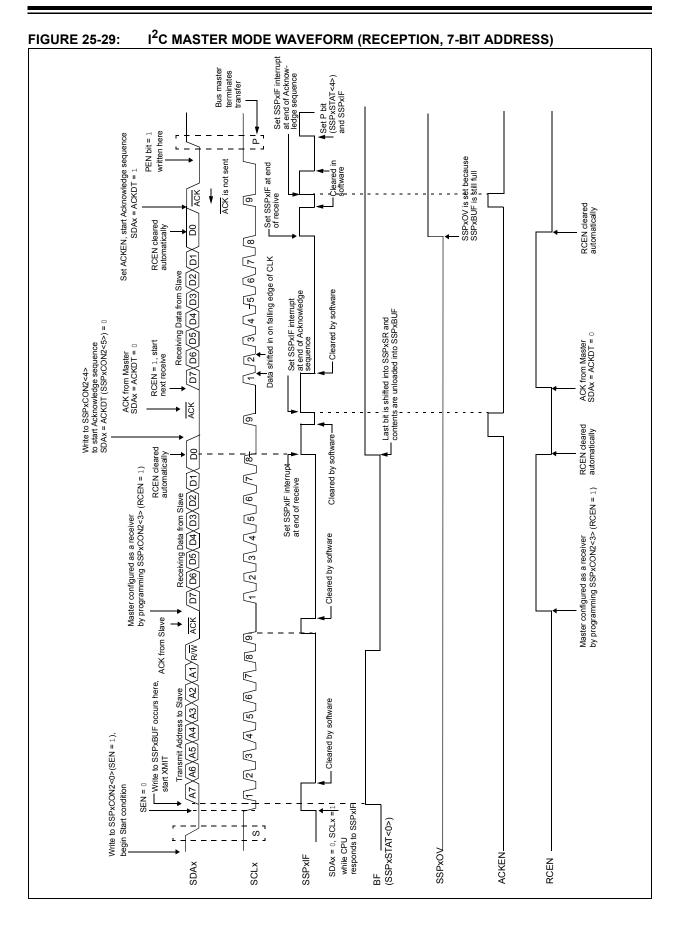
25.6.7.2 SSPxOV Status Flag

In receive operation, the SSPxOV bit is set when 8 bits are received into the SSPxSR and the BF flag bit is already set from a previous reception.

25.6.7.3 WCOL Status Flag

If the user writes the SSPxBUF when a receive is already in progress (i.e., SSPxSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur). 25.6.7.4 Typical Receive Sequence:

- 1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
- 2. SSPxIF is set by hardware on completion of the Start.
- 3. SSPxIF is cleared by software.
- 4. User writes SSPxBUF with the slave address to transmit and the R/W bit set.
- 5. Address is shifted out the SDAx pin until all 8 bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
- The MSSPx module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
- The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
- 8. User sets the RCEN bit of the SSPxCON2 register and the Master clocks in a byte from the slave.
- 9. After the 8th falling edge of SCLx, SSPxIF and BF are set.
- 10. Master clears SSPxIF and reads the received byte from SSPxUF, clears BF.
- Master sets ACK value sent to slave in ACKDT bit of the SSPxCON2 register and initiates the ACK by setting the ACKEN bit.
- 12. Masters ACK is clocked out to the slave and SSPxIF is set.
- 13. User clears SSPxIF.
- 14. Steps 8-13 are repeated for each received byte from the slave.
- 15. Master sends a not ACK or Stop to end communication.



25.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPxCON2 register. When this bit is set, the SCLx pin is pulled low and the contents of the Acknowledge data bit are presented on the SDAx pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCLx pin is deasserted (pulled high). When the SCLx pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCLx pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSPx module then goes into Idle mode (Figure 25-29).

25.6.8.1 WCOL Status Flag

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

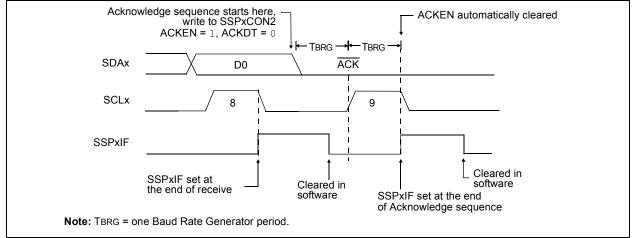
25.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDAx pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPxCON2 register. At the end of a receive/transmit, the SCLx line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDAx line low. When the SDAx line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCLx pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDAx pin will be deasserted. When the SDAx pin is sampled high while SCLx is high, the P bit of the SSPxSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPxIF bit is set (Figure 25-30).

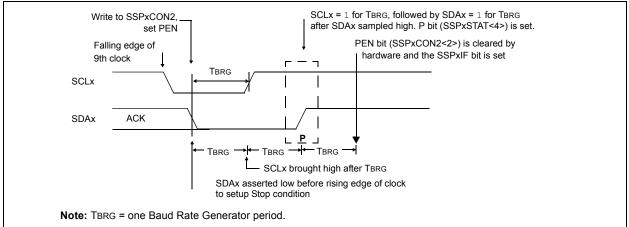
25.6.9.1 WCOL Status Flag

If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 25-30: ACKNOWLEDGE SEQUENCE WAVEFORM







25.6.10 SLEEP OPERATION

While in Sleep mode, the I²C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSPx interrupt is enabled).

25.6.11 EFFECTS OF A RESET

A Reset disables the MSSPx module and terminates the current transfer.

25.6.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSPx module is disabled. Control of the I²C bus may be taken when the P bit of the SSPxSTAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSPx interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDAx line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCLxIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

25.6.13 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDAx pin, arbitration takes place when the master outputs a '1' on SDAx, by letting SDAx float high and another master asserts a '0'. When the SCLx pin floats high, data should be stable. If the expected data on SDAx is a '1' and the data sampled on the SDAx pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLxIF and reset the I²C port to its Idle state (Figure 25-31).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDAx and SCLx lines are deasserted and the SSPxBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the l^2C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDAx and SCLx lines are deasserted and the respective control bits in the SSPxCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDAx and SCLx pins. If a Stop condition occurs, the SSPxIF bit will be set.

A write to the SSPxBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSPxSTAT register, or the bus is Idle and the S and P bits are cleared.

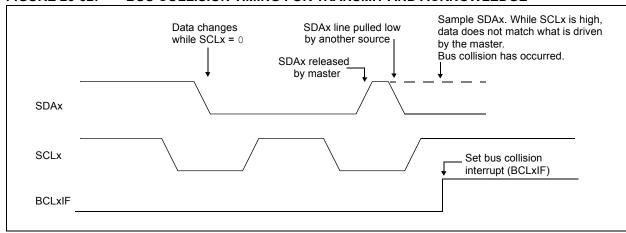


FIGURE 25-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE

25.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- a) SDAx or SCLx are sampled low at the beginning of the Start condition (Figure 25-32).
- b) SCLx is sampled low before SDAx is asserted low (Figure 25-33).

During a Start condition, both the SDAx and the SCLx pins are monitored.

If the SDAx pin is already low, or the SCLx pin is already low, then all of the following occur:

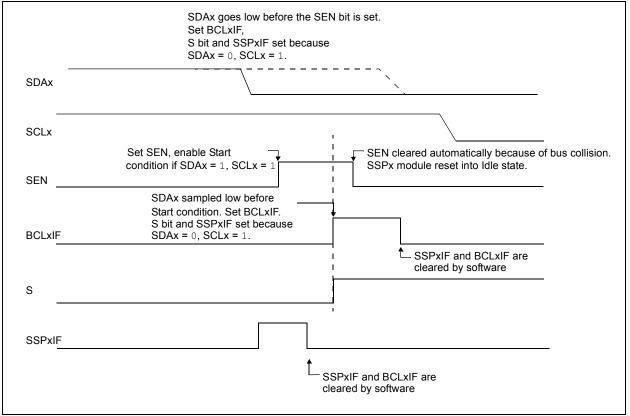
- · the Start condition is aborted,
- the BCLxIF flag is set and
- the MSSPx module is reset to its Idle state (Figure 25-32).

The Start condition begins with the SDAx and SCLx pins deasserted. When the SDAx pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCLx pin is sampled low while SDAx is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDAx pin is sampled low during this count, the BRG is reset and the SDAx line is asserted early (Figure 25-34). If, however, a '1' is sampled on the SDAx pin, the SDAx pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCLx pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCLx pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDAx before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

FIGURE 25-33: BUS COLLISION DURING START CONDITION (SDAX ONLY)





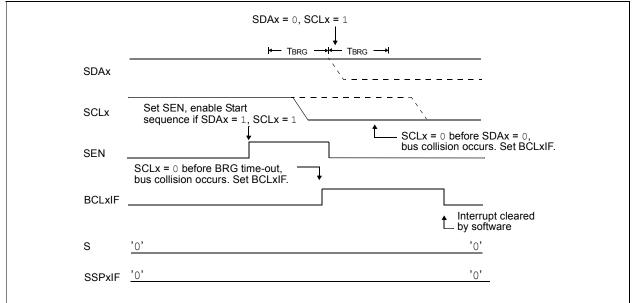
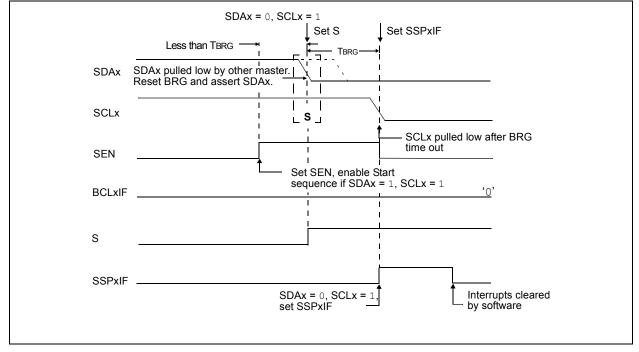


FIGURE 25-35: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION



25.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

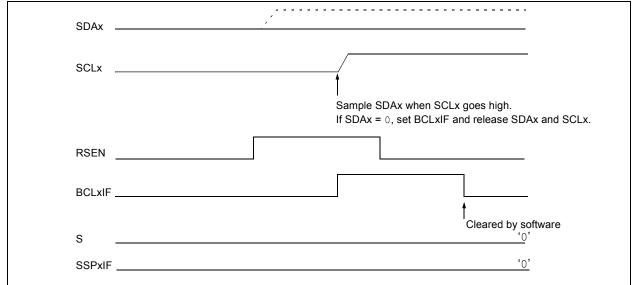
- a) A low level is sampled on SDAx when SCLx goes from low level to high level.
- SCLx goes low before SDAx is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user releases SDAx and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCLx pin is then deasserted and when sampled high, the SDAx pin is sampled. If SDAx is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 25-35). If SDAx is sampled high, the BRG is reloaded and begins counting. If SDAx goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDAx at exactly the same time.

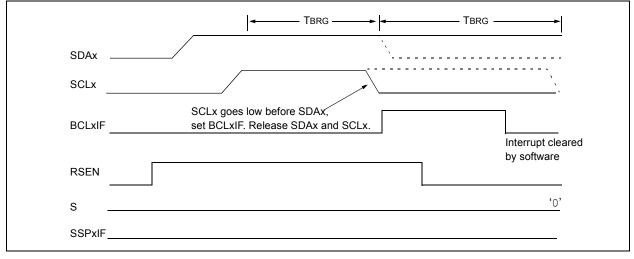
If SCLx goes from high-to-low before the BRG times out and SDAx has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 25-36.

If, at the end of the BRG time-out, both SCLx and SDAx are still high, the SDAx pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCLx pin, the SCLx pin is driven low and the Repeated Start condition is complete.

FIGURE 25-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)







25.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

- a) After the SDAx pin has been deasserted and allowed to float high, SDAx is sampled low after the BRG has timed out.
- b) After the SCLx pin is deasserted, SCLx is sampled low before SDAx goes high.

The Stop condition begins with SDAx asserted low. When SDAx is sampled low, the SCLx pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPxADD and counts down to 0. After the BRG times out, SDAx is sampled. If SDAx is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 25-37). If the SCLx pin is sampled low before SDAx is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 25-38).

FIGURE 25-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)

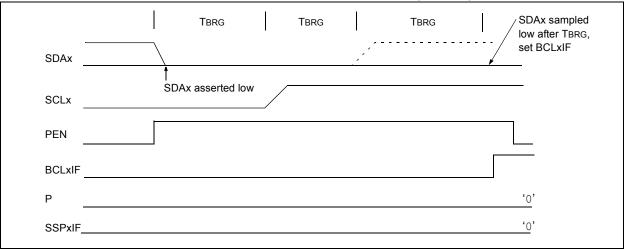
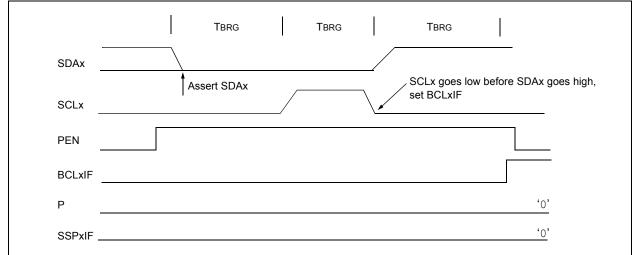


FIGURE 25-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)



Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INLVLA	_	_	INLVLA5 ⁽¹⁾	INLVLA4	INLVLA3 ⁽²⁾	INLVLA2	INLVLA1	INLVLA0	131
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	_	—	-	136
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3 ⁽²⁾	INLVLC2 ⁽²⁾	INLVLC1	INLVLC0	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	_	_	CCP2IE	95
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	_	_	CCP2IF	99
SSP1ADD	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	297
SSP1BUF	Synchronous	Serial Port Rece	eive Buffer/Trans	smit Register					249*
SSP1CON1	WCOL	SSPOV	SSPEN	СКР		SSPM	<3:0>		294
SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	295
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	296
SSP1MSK	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	297
SSP1STAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	293
TRISA	—	_	TRISA5 ⁽¹⁾	TRISA4	TRISA3 ⁽²⁾	TRISA2	TRISA1	TRISA0	129
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	—	_	_	_	135
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3(2)	TRISC2 ⁽²⁾	TRISC1	TRISC0	140

SUMMARY OF REGISTERS ASSOCIATED WITH I²C[™] OPERATION **TABLE 25-3:**

— = unimplemented location, read as '0'. Shaded cells are not used by the MSSP module in I²C[™] mode. Legend: Page provides register information. PIC16F/LF1829 only. PIC16F/LF1825 only.

Note 1:

2:

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25.7 BAUD RATE GENERATOR

The MSSPx module has a Baud Rate Generator available for clock generation in both I²C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPxADD register (Register 25-6). When a write occurs to SSPxBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

An internal signal "Reload" in Figure 25-39 triggers the value from SSPxADD to be loaded into the BRG counter. This occurs twice for each oscillation of the

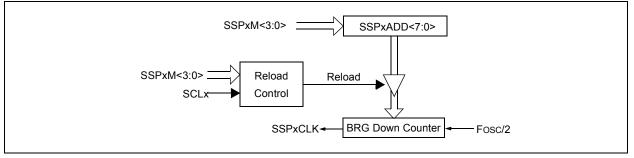
module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSPx is being operated in.

Table 25-4demonstratesclockratesbasedoninstructioncyclesandtheBRGvalueloadedintoSSPxADD.

EQUATION 25-1:

$$FCLOCK = \frac{FOSC}{(SSPxADD + 1)(4)}$$

FIGURE 25-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPxADD when used as a Baud Rate Generator for I²C. This is an implementation limitation.

TABLE 25-4: MSSPX CLOCK RATE W/BRG

Fosc	Fcy	BRG Value	FCLOCK (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz ⁽¹⁾
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz ⁽¹⁾
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note 1: The I²C interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

REGISTER 25-1: SSPxSTAT: SSPx STATUS REGISTER

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0			
SMP	CKE	D/A	Р	S	R/W	UA	BF			
bit 7							bit C			
Legend:										
R = Readable b	bit	W = Writable bi	t		ented bit, read as					
u = Bit is uncha	anged	x = Bit is unkno	wn	-n/n = Value at	POR and BOR/Va	alue at all other	Resets			
'1' = Bit is set		'0' = Bit is clear	ed							
bit 7	SMD: SDI Data	Innut Comple hi	4							
	SPI Master mo	Input Sample bi	L							
		sampled at end o	f data output tir	me						
	0 = Input data	sampled at middl	e of data outpu	t time						
	SMP must be of	<u>e:</u> cleared when SPI	is used in Slav	ve mode						
	In I ² C Master c			lindue						
	1 = Slew rate	control disabled f	or standard spe	eed mode (100 k	Hz and 1 MHz)					
	0 = Slew rate	control enabled f	or high speed n	node (400 kHz)						
bit 6		k Edge Select bit	(SPI mode onl	y)						
		In SPI Master or Slave mode:								
	 1 = Transmit occurs on transition from active to Idle clock state 0 = Transmit occurs on transition from Idle to active clock state 									
	In I ² C™ mode only:									
	 1 = Enable input logic so that thresholds are compliant with SMbus specification 0 = Disable SMbus specific inputs 									
		• •								
bit 5	D/A: Data/Address bit (I ² C mode only) 1 = Indicates that the last byte received or transmitted was data									
	0 = Indicates that the last byte received or transmitted was data									
bit 4	P: Stop bit	,								
	(I ² C mode only	(I ² C mode only. This bit is cleared when the MSSPx module is disabled, SSPxEN is cleared.)								
	1 = Indicates that a Stop bit has been detected last (this bit is '0' on Reset)									
	•	s not detected la	st							
bit 3	S: Start bit									
	(I ² C mode only. This bit is cleared when the MSSPx module is disabled, SSPxEN is cleared.)									
	 1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset) 0 = Start bit was not detected last 									
bit 2		te bit information		V)						
2.1.2					match. This bit is o	nly valid from the	e address match			
		t bit, Stop bit, or				-				
	1 = Read	ode.								
	0 = Write									
	In I ² C Master n									
		1 = Transmit is in progress 0 = Transmit is not in progress								
				CEN or ACKEN	will indicate if the I	MSSPx is in Idle	mode.			
bit 1	OR-ing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSPx is in Idle mode. UA: Update Address bit (10-bit I ² C mode only)									
		1 = Indicates that the user needs to update the address in the SSPxADD register								
		bes not need to b	e updated							
bit 0	BF: Buffer Full	-								
		nd I ² C modes): mplete, SSPxBU	E is full							
		of complete, SSPXBU								
	Transmit (I ² C n									
	1 = Data transr	nit in progress (d			top bits), SSPxBU					
	0 = Data transr	nit complete (doe	es not include th	ne ACK and Stop	o bits), SSPxBUF i	is empty				

REGISTER 25-2: SSPxCON1: SSPx CONTROL REGISTER 1

R/C/HS-0/	/0 R/C/HS-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WCOL	SSPxOV	SSPxEN	CKP		SSPx	M<3:0>	
bit 7							bit
Legend:							
R = Readable	e bit	W = Writable bit		•	ted bit, read as '0'		
u = Bit is uncl		x = Bit is unknow		-n/n = Value at P	OR and BOR/Value	at all other Resets	
'1' = Bit is set		'0' = Bit is cleared	1	HS = Bit is set by	hardware	C = User cleared	
bit 7	0 = No collisior <u>Slave mode:</u>	ne SSPxBUF regist 1 UF register is written	·	d while the I ² C cond smitting the previous		I for a transmission t ed in software)	to be started
bit 6	SSPxOV: Receiv In SPI mode: 1 = A new byte Overflow ca setting over SSPxBUF r 0 = No overflow In I ² C mode: 1 = A byte is received.	e Overflow Indicato is received while the in only occur in Slav flow. In Master mode egister (must be cleived v ceived while the St eared in software).	SSPxBUF registe e mode. In Slave e, the overflow bit ared in software).	mode, the user musi is not set since each	read the SSPxBUF, new reception (and t	of overflow, the data even if only transmit ransmission) is initiate OV is a "don't care"	ting data, to avoi ed by writing to th
bit 5	SSPxEN: Synchri In both modes, w In <u>SPI mode:</u> 1 = Enables see 0 = Disables see <u>In I²C mode:</u> 1 = Enables the	ronous Serial Port E rhen enabled, these rial port and configur erial port and config	e pins must be pr res SCKx, SDOx, ures these pins a igures the SDAx a	and SCLx pins as the	e source of the serial		
bit 4	CKP: Clock Pola <u>In SPI mode:</u> 1 = Idle state for 0 = Idle state for <u>In I²C Slave mod</u> SCLx release cou 1 = Enable clock	rity Select bit clock is a high leve clock is a low level <u>e:</u> ntrol pw (clock stretch). (de:					
bit 3-0	0000 = SPI Masi 0001 = SPI Masi 0010 = SPI Masi 0010 = SPI Masi 0100 = SPI Slav 0101 = SPI Slav 0101 = I ² C Slave 0111 = I ² C Slave 1000 = I ² C Masi 1001 = Reserved 1010 = SPI Masi 1011 = I ² C firmw 1100 = Reserved 1011 = Reserved 1101 = I ² C Slave	e mode, 7-bit addre: e mode, 10-bit addr er mode, clock = Fo ter mode, clock = Fo vare controlled Mast d d e mode, 7-bit addre:	osc/4 osc/16 osc/64 MR2 output/2 Kx pin, <u>SSx</u> pin iKx pin, <u>SSx</u> pin iKx pin, <u>SSx</u> pin iSx pi	control enabled control disabled, SS \DD+1)) ⁽⁴⁾ DD+1)) ⁽⁵⁾	nabled	O pin	
Note 1: 2: 3: 4:	In Master mode, the ov When enabled, these p When enabled, the SD/ SSPxADD values of 0,	erflow bit is not set ins must be properl Ax and SCLx pins n	since each new y configured as i nust be configure	reception (and trans nput or output. d as inputs.		by writing to the SS	PxBUF register

- 4: SSPxADD values of 0, 1 or 2 are not supported for I²C Mode.
 5: SSPxADD value of '0' is not supported. Use SSPxM = 0000 instead.

R/W-0/0	R-0/0	R/W-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/W/HS-0/0	
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	
bit 7			•				bit	
Legend:								
R = Readable		W = Writable		•	mented bit, read			
u = Bit is unch	anged	x = Bit is unk			at POR and BO		ther Resets	
'1' = Bit is set		'0' = Bit is cle	eared	HC = Cleared	d by hardware	S = User set		
bit 7	1 = Enable in		•	• •	or 00h) is receiv	ed in the SSPx	SR	
bit 6	1 = Acknowle	ACKSTAT: Acknowledge Status bit (in I ² C mode only) 1 = Acknowledge was not received 0 = Acknowledge was received						
bit 5	In Receive m	ode: itted when the owledge	a bit (in I ² C mo	• •	le sequence at	the end of a red	ceive	
bit 4	 ACKEN: Acknowledge Sequence Enable bit (in I²C Master mode only) <u>In Master Receive mode:</u> 1 = Initiate Acknowledge sequence on SDAx and SCLx pins, and transmit ACKD Automatically cleared by hardware. 0 = Acknowledge sequence Idle 					<dt b<="" data="" td=""></dt>		
bit 3		Receive mode	(in I ² C Master for I ² C	mode only)				
bit 2	SCKx Releas	e Control: op condition o	e bit (in I ² C Ma n SDAx and S(y) matically cleare	d by hardware.		
bit 1	 RSEN: Repeated Start Condition Enabled bit (in I²C Master mode only) 1 = Initiate Repeated Start condition on SDAx and SCLx pins. Automatically cleared by hardware. 0 = Repeated Start condition Idle 						y hardware.	
bit 0	<u>In Master mo</u> 1 = Initiate St 0 = Start cone	<u>de:</u> art condition o dition Idle	ed bit (in I ² C N n SDAx and S ⁱ		nly) matically cleare	d by hardware		
				ave transmit ar	nd slave receive	e (stretch enabl	ed)	
Note 1: For	bits ACKEN. F	RCEN. PEN. R	SEN. SEN: If t	he I ² C module	is not in the IdI	e mode. this bit	t mav not be	

REGISTER 25-3: SSPxCON2: SSPx CONTROL REGISTER 2

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I²C module is not in the Idle mode, this bit may not be set (no spooling) and the SSPxBUF may not be written (or writes to the SSPxBUF are disabled).

R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0		
ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN		
bit 7		•		•			bit (
Legend:									
R = Readable	e bit	W = Writable	bit	U = Unimple	mented bit, read	d as '0'			
u = Bit is unc	hanged	x = Bit is unk	nown	-n/n = Value	at POR and BO	R/Value at all c	other Resets		
'1' = Bit is set		'0' = Bit is cle	ared						
			e (1) (1)	- · · · ·	(3)				
bit 7		knowledge Tim		• •			N		
					e, set on 8 ^{⊤н} fal g edge of SCLx		LX CIOCK		
bit 6		Condition Interro	-						
		nterrupt on dete	•	•	,				
		ection interrupt							
bit 5	SCIE: Start C	Condition Interre	upt Enable bit ((I ² C mode onl)	y)				
		nterrupt on dete ection interrupt			ditions				
bit 4	BOEN: Buffe	er Overwrite En	able bit						
	In SPI Slave								
		1 = SSPxBUF updates every time that a new data byte is shifted in ignoring the BF bit							
		= If new byte is received with BF bit of the SSPxSTAT register already set, SSPxOV bit of the SSPxCON1 register is set, and the buffer is not updated							
			mode and SPI Master mode:						
		s ignored.							
	In I ² C Slave		ed and $\overline{\Lambda CK}$ is	annerated fo	or a received ad	dress/data byte	a ignoring the		
		e of the SSPxO			a received ad		e, ignoring the		
		PxBUF is only u			ar				
bit 3	SDAHT: SD/	Ax Hold Time S	election bit (I ² 0	C mode only)					
					ng edge of SCL				
bit 2					ng edge of SCL C Slave mode c				
DIL Z						•			
		f the PIR2 regis			en the module i	s outputting a	nign state, the		
		lave bus collisi		0					
		s collision inter		led					
bit 1	AHEN: Addr	ess Hold Enabl	e bit (l ² C Slave	e mode only)					
		•	• •		hing received a	address byte; (CKP bit of the		
		SSPxCON1 register will be cleared and the SCLx will be held low. 0 = Address holding is disabled							
		-							
bit 0		Hold Enable b		• •	data byte; slave	hardware clos	ure the CKD h		
		SPxCON1 regi			Gala Dyle, Sidve				
		ding is disabled							
Note 1: Fo	r daisv-chained	SPI operation:	allows the use	r to ignore all h	out the last recei	ved byte SSPx	OV is still set		
					ies to write the n				
о т.	-				dition data ation i	-			

REGISTER 25-4: SSPxCON3: SSPx CONTROL REGISTER 3

2: This bit has no effect in Slave modes that Start and Stop condition detection is explicitly listed as enabled.

3: The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is set.

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	
			MSK	<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit		W = Writable bit		U = Unimplemented bit, read as '0'				
u = Bit is unc	hanged	x = Bit is unknown		-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set	I	'0' = Bit is cleared						
bit 7-1	MSK<7:1>: Mask bits							
		The received address bit n is compared to SSPxADD <n> to detect I²C address match</n>						
0 = The received address bit n is not used to detect I ² C address match								
bit 0	MSK<0>: Mask bit for I ² C Slave mode, 10-bit Address							

REGISTER 25-5: SSPxMSK: SSPx MASK REGISTER

I ² C Slave mode, 10-bit address (SSPxM<3:0> = 0111 or 1111):	0
--	---

1 = The received address bit 0 is compared to SSPxADD<0> to detect I²C address match

0 = The received address bit 0 is not used to detect I²C address match

I²C Slave mode, 7-bit address, the bit is ignored

REGISTER 25-6: SSPxADD: MSSPx ADDRESS AND BAUD RATE REGISTER (I²C MODE)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
	ADD<7:0>						
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

Master mode:

bit 7-0	ADD<7:0>: Baud Rate Clock Divider bits
	SCLx pin clock period = ((ADD<7:0> + 1) *4)/Fosc

<u>10-Bit Slave mode — Most Significant Address byte:</u>

- bit 7-3 **Not used:** Unused for Most Significant Address byte. Bit state of this register is a "don't care". Bit pattern sent by master is fixed by I²C specification and must be equal to '11110'. However, those bits are compared by hardware and are not affected by the value in this register.
- bit 2-1 ADD<2:1>: Two Most Significant bits of 10-bit address
- bit 0 Not used: Unused in this mode. Bit state is a "don't care".

<u>10-Bit Slave mode — Least Significant Address byte:</u>

bit 7-0 ADD<7:0>: Eight Least Significant bits of 10-bit address

7-Bit Slave mode:

bit 0 Not used: Unused in this mode. Bit state is a "don't care".

NOTES:

26.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

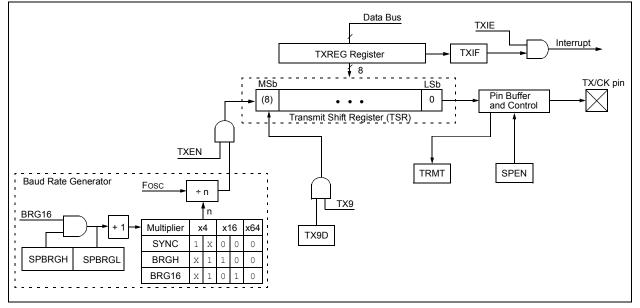
- · Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- · Programmable 8-bit or 9-bit character length
- · Address detection in 9-bit mode
- · Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- · Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- · Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- · 13-bit Break character transmit

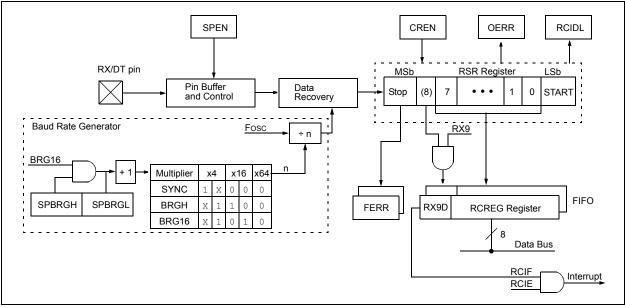
Block diagrams of the EUSART transmitter and receiver are shown in Figure 27-1 and Figure 27-2.

FIGURE 26-1: EUSART TRANSMIT BLOCK DIAGRAM



PIC16F/LF1825/1829

FIGURE 26-2: EUSART RECEIVE BLOCK DIAGRAM



The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These registers are detailed in Register 27-1, Register 27-2 and Register 27-3, respectively.

When the receiver or transmitter section is not enabled then the corresponding RX or TX pin may be used for general purpose input and output.

26.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH mark state which represents a '1' data bit, and a VOL space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is 8 bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 27-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

26.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 27-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

26.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

Note 1: The TXIF Transmitter Interrupt flag is set when the TXEN enable bit is set.

26.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one TCY immediately following the Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

26.1.1.3 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.

26.1.1.4 TSR Status

The TRMT bit of the TXSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note:	The TSR register is not mapped in data
	memory, so it is not available to the user.

26.1.1.5 Transmitting 9-Bit Characters

The EUSART supports 9-bit character transmissions. When the TX9 bit of the TXSTA register is set, the EUSART will shift 9 bits out for each character transmitted. The TX9D bit of the TXSTA register is the ninth, and Most Significant, data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the 8 Least Significant bits into the TXREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXREG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 27.1.2.7** "Address **Detection**" for more information on the address mode.

- 26.1.1.6 Asynchronous Transmission Set-up:
- 1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.3 "EUSART Baud Rate Generator (BRG)").
- 2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
- 3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the 8 Least Significant data bits are an address when the receiver is set for address detection.
- 4. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
- If interrupts are desired, set the TXIE interrupt enable bit of the PIE1 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
- 7. Load 8-bit data into the TXREG register. This will start the transmission.

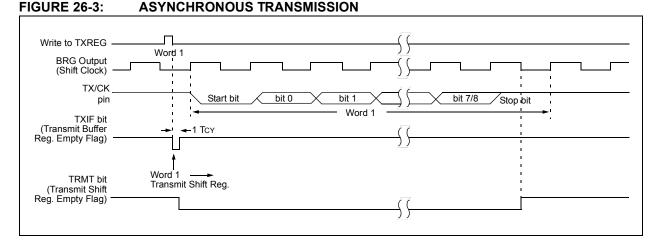
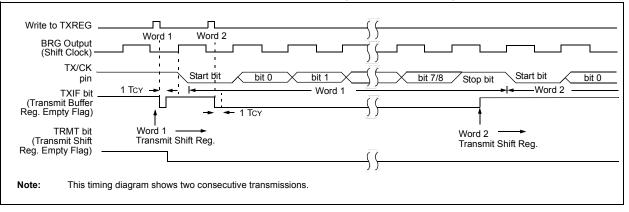


FIGURE 26-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)



Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	SDOSEL ⁽²⁾	SSSEL ⁽²⁾	_	T1GSEL	TXCKSEL	_	_	125
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	310
INLVLA ⁽³⁾	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	_	_	_	_	136
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	309
SPBRGL				BRG	<7:0>				311*
SPBRGH				BRG<	:15:8>				311*
TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	_	_	_	_	135
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140
TXREG	EUSART Tra	nsmit Data Re	egister						301
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	308

TABLE 26-1: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Asynchronous Transmission.
* Page provides register information.

Note 1: PIC16F/LF1829 only.

2: PIC16F/LF1825 only.

3: Unshaded cells apply to PIC16F/LF1825 only.

26.1.2 EUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 27-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all 8 or 9 bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the EUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREG register.

26.1.2.1 Enabling the Receiver

The EUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTA register enables the receiver circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART. The programmer must set the corresponding TRIS bit to configure the RX/DT I/O pin as an input.

Note 1: If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

26.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. See Section 27.1.2.4 "Receive Framing Error" for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the EUSART receive FIFO and the RCIF interrupt flag bit of the PIR1 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREG register.

characters condition is			
"Receive information		for	more

26.1.2.3 Receive Interrupts

The RCIF interrupt flag bit of the PIR1 register is set whenever the EUSART receiver is enabled and there is an unread character in the receive FIFO. The RCIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCIF interrupts are enabled by setting all of the following bits:

- · RCIE interrupt enable bit of the PIE1 register
- PEIE Peripheral Interrupt Enable bit of the INTCON register
- GIE Global Interrupt Enable bit of the INTCON register

The RCIF interrupt flag bit will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

26.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the EUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note:	If all receive characters in the receive
	FIFO have framing errors, repeated reads
	of the RCREG will not clear the FERR bit.

26.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by resetting the EUSART by clearing the SPEN bit of the RCSTA register.

26.1.2.6 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift 9 bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the 8 Least Significant bits from the RCREG.

26.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

26.1.2.8 Asynchronous Reception Set-up:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.3 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- 4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit reception is desired, set the RX9 bit.
- 6. Enable reception by setting the CREN bit.
- 7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
- 9. Get the received 8 Least Significant data bits from the receive buffer by reading the RCREG register.
- 10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

26.1.2.9 9-bit Address Detection Mode Set-up

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.3 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. Enable 9-bit reception by setting the RX9 bit.
- 6. Enable address detection by setting the ADDEN bit.
- 7. Enable reception by setting the CREN bit.
- The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 9. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
- 10. Get the received 8 Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
- 11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
- 12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

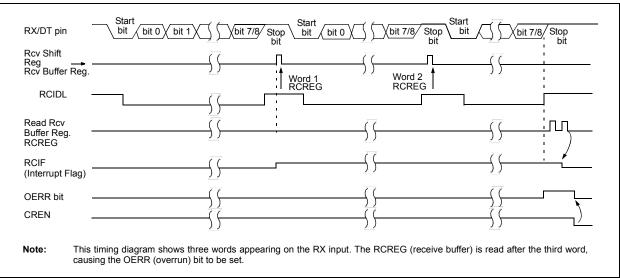


FIGURE 26-5: ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	SDOSEL ⁽²⁾	SSSEL ⁽²⁾	_	T1GSEL	TXCKSEL	_	—	125
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	310
INLVLA ⁽³⁾	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	_	_	_	—	136
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
RCREG			EU	ISART Receiv	ve Data Regis	ter			304*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	309
SPBRGL				BRG∢	<7:0>				311*
SPBRGH				BRG<	15:8>				311*
TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	_	—	_	—	135
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	308

TABLE 26-2: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Asynchronous Reception.

* Page provides register information.

Note 1: PIC16F/LF1829 only.

2: PIC16F/LF1825 only.

3: Unshaded cells apply to PIC16F/LF1825 only.

26.2 **Clock Accuracy with Asynchronous Operation**

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as VDD or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source. See Section 6.2.2 "Internal Clock Sources" for more information.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see Section 27.3.1 "Auto-Baud Detect"). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

REGISTER 26-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN ⁽¹⁾	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0
<u> </u>							
Legend:							
R = Readable	bit	W = Writable b	t	•	ented bit, read as		
u = Bit is unch	0	x = Bit is unkno		-n/n = Value at	POR and BOR/Va	alue at all other	Resets
'1' = Bit is set		'0' = Bit is clear	ed				
bit 7	CSRC: Clock	Source Select bit					
	Asynchronous	<u>s mode</u> :					
	Don't care						
	Synchronous			fram DDO)			
		node (clock gene ode (clock from e		from BRG)			
bit 6	TX9: 9-bit Tra	nsmit Enable bit					
		9-bit transmission 8-bit transmission					
bit 5		o-bit transmission nit Enable bit ⁽¹⁾					
DIL 5	1 = Transmit						
	0 = Transmit						
bit 4	SYNC: EUSA	RT Mode Select b	bit				
	1 = Synchror						
	0 = Asynchro						
bit 3		d Break Character	bit				
	Asynchronous		transmission (c	leared by bardwa	are upon completio	a n)	
		ak transmission o				511)	
	Synchronous	mode:					
	Don't care						
bit 2	0	Baud Rate Select	bit				
	Asynchronous						
	1 = High spe 0 = Low spee						
	Synchronous						
	Unused in this	s mode					
bit 1	TRMT: Transm	nit Shift Register S	Status bit				
	1 = TSR emp	oty					
h # 0	0 = TSR full		-				
bit 0		oit of Transmit Dat					
	Can be addres	ss/data bit or a pa	nty Dit.				
Note 1: S	REN/CREN overri	des TXFN in Svn	c mode				

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-x/x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit C
Legend:							
R = Readable		W = Writable	bit	•	mented bit, read		
u = Bit is unch	-	x = Bit is unk	nown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is cle	ared				
bit 7	SPEN: Seria	I Port Enable b	t				
		ort enabled (cor		F and TX/CK p	ins as serial po	rt pins)	
		ort disabled (he	-			()	
bit 6	RX9: 9-bit R	eceive Enable b	bit				
		9-bit reception 8-bit reception					
bit 5	SREN: Singl	le Receive Enal	ole bit				
	Asynchronou	<u>us mode</u> :					
	Don't care						
	•	<u>s mode – Maste</u>	<u>r</u> :				
		single receive					
		s single receive eared after rece	ntion is comple	ete			
		s mode – Slave					
	Don't care						
bit 4	CREN: Cont	inuous Receive	Enable bit				
	<u>Asynchronou</u>	<u>us mode</u> :					
	1 = Enables						
	0 = Disables						
	Synchronous		aiva until anak		algored (CDC		
		s continuous rec s continuous rec				N OVERTICES SRI	
bit 3	ADDEN: Add	dress Detect Er	able bit				
	<u>Asynchronou</u>	us mode 9-bit (F	<u>RX9 = 1)</u> :				
		address detect					
		s address detec		are received a	nd ninth bit can	be used as pa	rity bit
	•	<u>us mode 8-bit (F</u>	RX9 = 0):				
	Don't care	. –					
bit 2	FERR: Fram	•					L (.)
	1 = Framing 0 = No fram	ι error (can be ι ing error	ipdated by rea	aing RCREG r	register and rec	eive next valid	byte)
bit 1	OERR: Over	rrun Error bit					
	1 = Overrun 0 = No over	error (can be c run error	leared by clea	ring bit CREN))		
bit 0	RX9D: Ninth	bit of Received	Data				
	This can be a						

REGISTER 26-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER⁽¹⁾

R-0/0	R-1/1	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0
ABDOVF	RCIDL		SCKP	BRG16		WUE	ABDEN
bit 7	·				•		bit 0
Legend:							
R = Readable	bit	W = Writable	e bit	U = Unimple	mented bit, reac	l as '0'	
u = Bit is unch	nanged	x = Bit is unk	nown	-n/n = Value	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is set		'0' = Bit is cle	eared				
bit 7			ct Overflow bit				
	Asynchronou	<u>s mode</u> : d timer overflo	wed				
		d timer did not					
	Synchronous						
	Don't care						
bit 6	RCIDL: Rece	eive Idle Flag b	oit				
	Asynchronou						
	1 = Receiver		ved and the re	caivar is racai	<i>i</i> ng		
	Synchronous				ling		
	Don't care						
bit 5	Unimplemen	ted: Read as	' O '				
bit 4	SCKP: Synch	nronous Clock	Polarity Select	t bit			
	<u>Asynchronou</u>	<u>s mode</u> :					
			to the TX/CK p lata to the TX/				
	<u>Synchronous</u>						
			g edge of the one of t				
bit 3		it Baud Rate (• •				
		ud Rate Gene Id Rate Gener					
bit 2	Unimplemen	ted: Read as	' 0 '				
bit 1	WUE: Wake-	up Enable bit					
	<u>Asynchronou</u>						
					will be received	, byte RCIF wil	l be set. WUE
		is operating n	after RCIF is se ormally	51.			
	Synchronous		ormany				
	Don't care						
bit 0	ABDEN: Auto	p-Baud Detect	Enable bit				
	<u>Asynchronou</u>	<u>s mode</u> :					
				clears when au	ito-baud is com	olete)	
		ud Detect mod	e is disabled				
	<u>Synchronous</u>	mode:					

REGISTER 26-3: BAUDCON: BAUD RATE CONTROL REGISTER

26.3 EUSART Baud Rate Generator (BRG)

The Baud Rate Generator (BRG) is an 8-bit or 16-bit timer that is dedicated to the support of both the asynchronous and synchronous EUSART operation. By default, the BRG operates in 8-bit mode. Setting the BRG16 bit of the BAUDCON register selects 16-bit mode.

The SPBRGH, SPBRGL register pair determines the period of the free running baud rate timer. In Asynchronous mode the multiplier of the baud rate period is determined by both the BRGH bit of the TXSTA register and the BRG16 bit of the BAUDCON register. In Synchronous mode, the BRGH bit is ignored.

Table 27-3 contains the formulas for determining the baud rate. Example 27-1 provides a sample calculation for determining the baud rate and baud rate error.

Typical baud rates and error values for various asynchronous modes have been computed for your convenience and are shown in Table 27-3. It may be advantageous to use the high baud rate (BRGH = 1), or the 16-bit BRG (BRG16 = 1) to reduce the baud rate error. The 16-bit BRG mode is used to achieve slow baud rates for fast oscillator frequencies.

Writing a new value to the SPBRGH, SPBRGL register pair causes the BRG timer to be reset (or cleared). This ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

If the system clock is changed during an active receive operation, a receive error or data loss may result. To avoid this problem, check the status of the RCIDL bit to make sure that the receive operation is Idle before changing the system clock.

EXAMPLE 26-1: CALCULATING BAUD RATE ERROR

For a device with Fosc of 16 MHz, desired baud rate of 9600, Asynchronous mode, 8-bit BRG:

Desired Baud Rate = $\frac{FOSC}{64([SPBRGH:SPBRGL] + 1)}$

Solving for SPBRGH:SPBRGL:

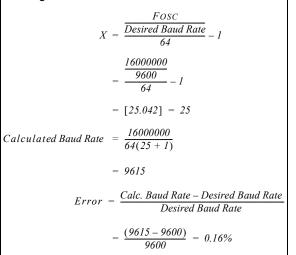


TABLE 26-3: BAUD RATE FORMULAS

C	onfiguration Bi	ts		David Data Farmula
SYNC	BRG16	BRGH	BRG/EUSART Mode	Baud Rate Formula
0	0	0	8-bit/Asynchronous	Fosc/[64 (n+1)]
0	0	1	8-bit/Asynchronous	
0	1	0	16-bit/Asynchronous	Fosc/[16 (n+1)]
0	1	1	16-bit/Asynchronous	
1	0	х	8-bit/Synchronous	Fosc/[4 (n+1)]
1	1	х	16-bit/Synchronous	

Legend: x = Don't care, n = value of SPBRGH, SPBRGL register pair.

TABLE 26-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page	
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	_	WUE	ABDEN	310	
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	309	
SPBRGL				BRG	<7:0>				311*	
SPBRGH	BRG<15:8>									
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	308	

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for the Baud Rate Generator.

* Page provides register information.

					SYNC	; = 0, BRG	I = 0, BRO	616 = 0				
BAUD	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	_	_	_	_		_	_	_	_	_	_	_
1200	—	—	—	1221	1.73	255	1200	0.00	239	1200	0.00	143
2400	2404	0.16	207	2404	0.16	129	2400	0.00	119	2400	0.00	71
9600	9615	0.16	51	9470	-1.36	32	9600	0.00	29	9600	0.00	17
10417	10417	0.00	47	10417	0.00	29	10286	-1.26	27	10165	-2.42	16
19.2k	19.23k	0.16	25	19.53k	1.73	15	19.20k	0.00	14	19.20k	0.00	8
57.6k	55.55k	-3.55	3	—	_	_	57.60k	0.00	7	57.60k	0.00	2
115.2k	—	_	_	_	_	_	—	_	_	—	_	—

TABLE 26-5: BAUD RATES FOR ASYNCHRONOUS MODES

					SYNC	; = 0, BRGH	I = 0, BRG	616 = 0				
BAUD	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300		_	_	300	0.16	207	300	0.00	191	300	0.16	51
1200	1202	0.16	103	1202	0.16	51	1200	0.00	47	1202	0.16	12
2400	2404	0.16	51	2404	0.16	25	2400	0.00	23	—	_	_
9600	9615	0.16	12	_	_	_	9600	0.00	5	—	_	_
10417	10417	0.00	11	10417	0.00	5	_	_	_	_	_	_
19.2k	_	_	_	_	_	_	19.20k	0.00	2	_	_	_
57.6k	—	_	—	—	—	—	57.60k	0.00	0	—	_	—
115.2k	—	_	—	—	_	—	—	_	—	—	_	—

					SYNC	C = 0, BRG	l = 1, BRO	G16 = 0				
BAUD	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—			—		—	—		—	_
1200	_	_	—	_		—	_	_	—	_	_	—
2400		_	_	_	_	_	_	_	_	_	_	_
9600	9615	0.16	207	9615	0.16	129	9600	0.00	119	9600	0.00	71
10417	10417	0.00	191	10417	0.00	119	10378	-0.37	110	10473	0.53	65
19.2k	19.23k	0.16	103	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35
57.6k	57.14k	-0.79	34	56.82k	-1.36	21	57.60k	0.00	19	57.60k	0.00	11
115.2k	117.64k	2.12	16	113.64k	-1.36	10	115.2k	0.00	9	115.2k	0.00	5

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					SYNC	; = 0, BRG	I = 1, BRO	616 = 0				
BAUD	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	_	_	_	_	_	_	_		_	300	0.16	207
1200	—	_	—	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—		—
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19231	0.16	25	19.23k	0.16	12	19.2k	0.00	11	_	_	_
57.6k	55556	-3.55	8	—	_	_	57.60k	0.00	3	—	_	_
115.2k	—	_	_	—	_	_	115.2k	0.00	1	—	_	—

TABLE 26-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

					SYNC	; = 0, BRG	I = 0, BRO	616 = 1					
BAUD	Foso	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	
300	300.0	0.00	6666	300.0	-0.01	4166	300.0	0.00	3839	300.0	0.00	2303	
1200	1200	-0.02	3332	1200	-0.03	1041	1200	0.00	959	1200	0.00	575	
2400	2401	-0.04	832	2399	-0.03	520	2400	0.00	479	2400	0.00	287	
9600	9615	0.16	207	9615	0.16	129	9600	0.00	119	9600	0.00	71	
10417	10417	0.00	191	10417	0.00	119	10378	-0.37	110	10473	0.53	65	
19.2k	19.23k	0.16	103	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35	
57.6k	57.14k	-0.79	34	56.818	-1.36	21	57.60k	0.00	19	57.60k	0.00	11	
115.2k	117.6k	2.12	16	113.636	-1.36	10	115.2k	0.00	9	115.2k	0.00	5	

					SYNC	= 0, BRGH	I = 0, BRC	616 = 1				
BAUD	Fosc = 8.000) MHz	Fos	c = 4.000) MHz	Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	299.9	-0.02	1666	300.1	0.04	832	300.0	0.00	767	300.5	0.16	207
1200	1199	-0.08	416	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	_	_	_
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19.23k	0.16	25	19.23k	0.16	12	19.20k	0.00	11	_	_	_
57.6k	55556	-3.55	8	—	_	_	57.60k	0.00	3	—	_	_
115.2k	—	_	_	—	_	_	115.2k	0.00	1	—	_	_

				SYNC = 0	, BRGH	= 1, BRG16	= 1 or SY	(NC = 1,	BRG16 = 1			
BAUD	Foso	Fosc = 32.000 MHz			= 20.00	0 MHz	Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287
10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23

TABLE 26-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

				SYNC = 0	, BRGH	= 1, BRG16	= 1 or SY	'NC = 1,	BRG16 = 1			
BAUD	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	_	_
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—

26.3.1 AUTO-BAUD DETECT

The EUSART module supports automatic detection and calibration of the baud rate.

In the Auto-Baud Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. The Baud Rate Generator is used to time the period of a received 55h (ASCII "U") which is the Sync character for the LIN bus. The unique feature of this character is that it has five rising edges including the Stop bit edge.

Setting the ABDEN bit of the BAUDCON register starts the auto-baud calibration sequence (Figure 27-6). While the ABD sequence takes place, the EUSART state machine is held in Idle. On the first rising edge of the receive line, after the Start bit, the SPBRG begins counting up using the BRG counter clock as shown in Table 27-6. The fifth rising edge will occur on the RX pin at the end of the eighth bit period. At that time, an accumulated value totaling the proper BRG period is left in the SPBRGH, SPBRGL register pair, the ABDEN bit is automatically cleared and the RCIF interrupt flag is set. The value in the RCREG needs to be read to clear the RCIF interrupt. RCREG content should be discarded. When calibrating for modes that do not use the SPBRGH register the user can verify that the SPBRGL register did not overflow by checking for 00h in the SPBRGH register.

The BRG auto-baud clock is determined by the BRG16 and BRGH bits as shown in Table 27-6. During ABD, both the SPBRGH and SPBRGL registers are used as a 16-bit counter, independent of the BRG16 bit setting. While calibrating the baud rate period, the SPBRGH and SPBRGL registers are clocked at 1/8th the BRG base clock rate. The resulting byte measurement is the average bit time when clocked at full speed.

- Note 1: If the WUE bit is set with the ABDEN bit, auto-baud detection will occur on the byte following the Break character (see Section 27.3.3 "Auto-Wake-up on Break").
 - It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible.
 - 3: During the auto-baud process, the auto-baud counter starts counting at 1. Upon completion of the auto-baud sequence, to achieve maximum accuracy, subtract 1 from the SPBRGH:SPBRGL register pair.

	TABLE 26-6:	BRG COUNTER CLOCK RATES
--	-------------	-------------------------

BRG16	BRGH	BRG Base Clock	BRG ABD Clock
0	0	Fosc/64	Fosc/512
0	1	Fosc/16	Fosc/128
1	0	Fosc/16	Fosc/128
1	1	Fosc/4	Fosc/32

Note: During the ABD sequence, SPBRGL and SPBRGH registers are both used as a 16-bit counter, independent of BRG16 setting.

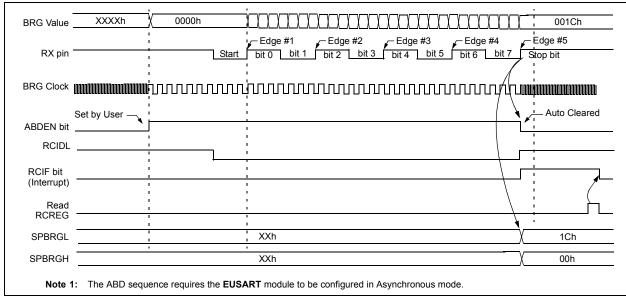


FIGURE 26-6: AUTOMATIC BAUD RATE CALIBRATION

26.3.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPBRGH:SPBRGL register pair. After the ABDOVF has been set, the counter continues to count until the fifth rising edge is detected on the RX pin. Upon detecting the fifth RX edge, the hardware will set the RCIF interrupt flag and clear the ABDEN bit of the BAUDCON register. The RCIF flag can be subsequently cleared by reading the RCREG register. The ABDOVF flag of the BAUDCON register can be cleared by software directly.

To terminate the auto-baud process before the RCIF flag is set, clear the ABDEN bit then clear the ABDOVF bit of the BAUDCON register. The ABDOVF bit will remain set if the ABDEN bit is not cleared first.

26.3.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDCON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 27-7), and asynchronously if the device is in Sleep mode (Figure 27-8). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

26.3.3.1 Special Considerations

Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be 10 or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

Oscillator Start-up Time

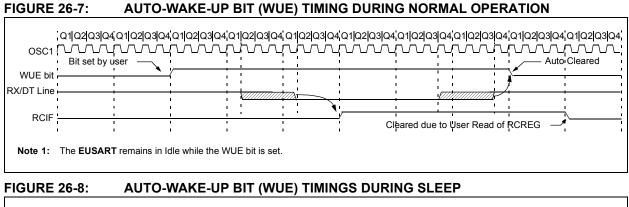
Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

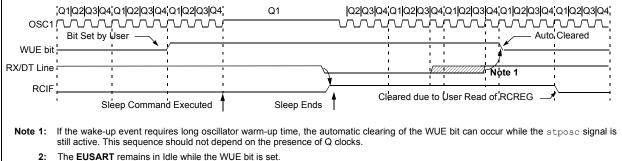
<u>WUE Bit</u>

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RCREG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

PIC16F/LF1825/1829





26.3.4 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. A Break character consists of a Start bit, followed by 12 '0' bits and a Stop bit.

To send a Break character, set the SENDB and TXEN bits of the TXSTA register. The Break character transmission is then initiated by a write to the TXREG. The value of data written to TXREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

The TRMT bit of the TXSTA register indicates when the transmit operation is active or Idle, just as it does during normal transmission. See Figure 27-9 for the timing of the Break character sequence.

26.3.4.1 Break and Sync Transmit Sequence

The following sequence will start a message frame header made up of a Break, followed by an auto-baud Sync byte. This sequence is typical of a LIN bus master.

- 1. Configure the EUSART for the desired mode.
- 2. Set the TXEN and SENDB bits to enable the Break sequence.
- 3. Load the TXREG with a dummy character to initiate transmission (the value is ignored).
- 4. Write '55h' to TXREG to load the Sync character into the transmit FIFO buffer.
- 5. After the Break has been sent, the SENDB bit is reset by hardware and the Sync character is then transmitted.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

FIGURE 26-9: SEND BREAK CHARACTER SEQUENCE Write to TXREG -Dummy Write **BRG** Output (Shift Clock) TX (pin) Start bit bit 0 bit 1 Stop bit Break TXIF bit (Transmit Interrupt Flag) TRMT bit (Transmit Shift Empty Flag) SENDB Sampled Here Auto Cleared SENDB (send Break control bit)

26.3.5 RECEIVING A BREAK CHARACTER

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RCSTA register and the Received data as indicated by RCREG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

A Break character has been received when;

- RCIF bit is set
- FERR bit is set
- RCREG = 00h

The second method uses the Auto-Wake-up feature described in **Section 27.3.3** "**Auto-Wake-up on Break**". By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUDCON register before placing the EUSART in Sleep mode.

26.4 EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

26.4.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for Synchronous Master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the EUSART.

26.4.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

26.4.1.2 Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the SCKP bit of the BAUDCON register. Setting the SCKP bit sets the clock Idle state as high. When the SCKP bit is set, the data changes on the falling edge of each clock. Clearing the SCKP bit sets the Idle state as low. When the SCKP bit is cleared, the data changes on the rising edge of each clock.

26.4.1.3 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note:	The TSR register is not mapped in data
	memory, so it is not available to the user.

- 26.4.1.4 Synchronous Master Transmission Set-up:
- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.3 "EUSART Baud Rate Generator (BRG)").
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. Disable Receive mode by clearing bits SREN and CREN.
- 4. Enable Transmit mode by setting the TXEN bit.
- 5. If 9-bit transmission is desired, set the TX9 bit.
- 6. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
- 8. Start transmission by loading data to the TXREG register.

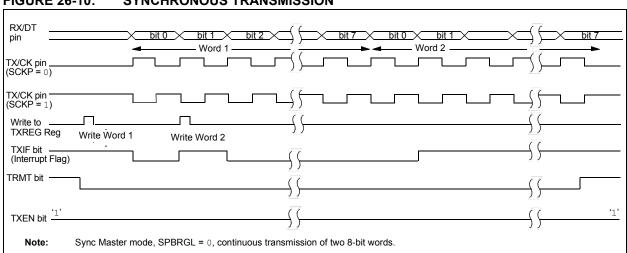


FIGURE 26-10: SYNCHRONOUS TRANSMISSION



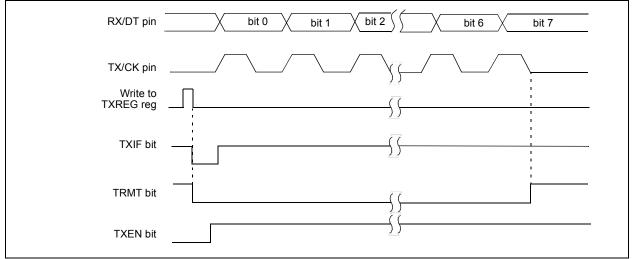


TABLE 26-7: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	SDOSEL ⁽¹⁾	SSSEL ⁽¹⁾	_	T1GSEL	TXCKSEL	—	—	125
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	310
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	309
SPBRGL				BRG	<7:0>				311*
SPBRGH				BRG<	:15:8>				311*
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140
TXREG	EUSART Transmit Data Register								301*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	308

- = unimplemented location, read as '0'. Shaded cells are not used for Synchronous Master Transmission. Legend:

Page provides register information. PIC16F/LF1825 only.

Note 1:

26.4.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

Note:	If the RX/DT function is on an analog pin,
	the corresponding ANSEL bit must be
	cleared for the receiver to function.

26.4.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

Note: If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.

26.4.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

26.4.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift 9-bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the 8 Least Significant bits from the RCREG.

26.4.1.9 Synchronous Master Reception Set-up:

- 1. Initialize the SPBRGH, SPBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- 3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 4. Ensure bits CREN and SREN are clear.
- 5. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 6. If 9-bit reception is desired, set bit RX9.
- 7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
- 8. Interrupt flag bit RCIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 10. Read the 8-bit received data by reading the RCREG register.
- 11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

PIC16F/LF1825/1829

FIGURE 26-12:	SYNCHRONOUS RECEPTION (MASTER MODE, SREN)
RX/DT pin TX/CK pin (SCKP = 0)	
TX/CK pin	
SREN bit	·
CREN bit <u>'0'</u> RCIF bit (Interrupt)	
Read RCREG	gram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

TABLE 26-8:SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER
RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	SDOSEL ⁽¹⁾	SSSEL ⁽¹⁾	—	T1GSEL	TXCKSEL	—	—	125
BAUDCON	ABDOVF	RCIDL	1	SCKP	BRG16	—	WUE	ABDEN	310
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
RCREG	EUSART Receive Data Register								304*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	309
SPBRGL	BRG<7:0>								311*
SPBRGH	BRG<15:8>							311*	
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	308

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Synchronous Master Reception.
* Page provides register information.

Note 1: PIC16F/LF1825 only.

26.4.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the EUSART for Synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the EUSART.

26.4.2.1 EUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (see Section 27.4.1.3 "Synchronous Master Transmission"), except in the case of the Sleep mode. If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- 1. The first character will immediately transfer to the TSR register and transmit.
- 2. The second word will remain in TXREG register.
- 3. The TXIF bit will not be set.
- After the first character has been shifted out of TSR, the TXREG register will transfer the second character to the TSR and the TXIF bit will now be set.
- If the PEIE and TXIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.
- 26.4.2.2 Synchronous Slave Transmission Set-up:
- 1. Set the SYNC and SPEN bits and clear the CSRC bit.
- 2. Clear the ANSEL bit for the CK pin (if applicable).
- 3. Clear the CREN and SREN bits.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit transmission is desired, set the TX9 bit.
- 6. Enable transmission by setting the TXEN bit.
- 7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
- 8. Start transmission by writing the Least Significant 8 bits to the TXREG register.

TABLE 26-9: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	SDOSEL ⁽¹⁾	SSSEL ⁽¹⁾	_	T1GSEL	TXCKSEL	_	—	125
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	310
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	309
TXREG	EUSART Transmit Data Register								301*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	308

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Synchronous Slave Transmission.
 * Page provides register information.

Note 1: PIC16F/LF1825 only.

26.4.2.3 EUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (Section 27.4.1.5 "Synchronous Master Reception"), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never Idle
- SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE enable bit is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

- 26.4.2.4 Synchronous Slave Reception Set-up:
- 1. Set the SYNC and SPEN bits and clear the CSRC bit.
- 2. Clear the ANSEL bit for both the CK and DT pins (if applicable).
- 3. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 4. If 9-bit reception is desired, set the RX9 bit.
- 5. Set the CREN bit to enable reception.
- The RCIF bit will be set when reception is complete. An interrupt will be generated if the RCIE bit was set.
- 7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
- 8. Retrieve the 8 Least Significant bits from the receive FIFO by reading the RCREG register.
- 9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

TABLE 26-10: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	SDOSEL ⁽¹⁾	SSSEL ⁽¹⁾	—	T1GSEL	TXCKSEL	_	—	125
BAUDCON	ABDOVF	RCIDL	-	SCKP	BRG16	—	WUE	ABDEN	310
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	94
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
RCREG	EUSART Receive Data Register								304*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	309
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	308

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Synchronous Slave Reception.

* Page provides register information.

Note 1: PIC16F/LF1825 only.

26.5 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

26.5.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see Section 27.4.2.4 "Synchronous Slave Reception Set-up").
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE, Global Interrupt Enable, bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

26.5.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Transmission (see Section 27.4.2.2 "Synchronous Slave Transmission Set-up").
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

26.5.3 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function registers, APFCON0 and APFCON1. To determine which pins can be moved and what their default locations are upon a Reset, see Section 12.1 "Alternate Pin Function" for more information.

27.0 CAPACITIVE SENSING (CPS) MODULE

The Capacitive Sensing (CPS) module allows for an interaction with an end user without a mechanical interface. In a typical application, the CPS module is attached to a pad on a Printed Circuit Board (PCB), which is electrically isolated from the end user. When the end user places their finger over the PCB pad, a capacitive load is added, causing a frequency shift in the CPS module. The CPS module requires software and at least one timer resource to determine the change in frequency. Key features of this module include:

- · Analog MUX for monitoring multiple inputs
- · Capacitive sensing oscillator
- · Multiple Power modes
- · High power range with variable voltage references
- · Multiple timer resources
- Software control
- · Operation during Sleep

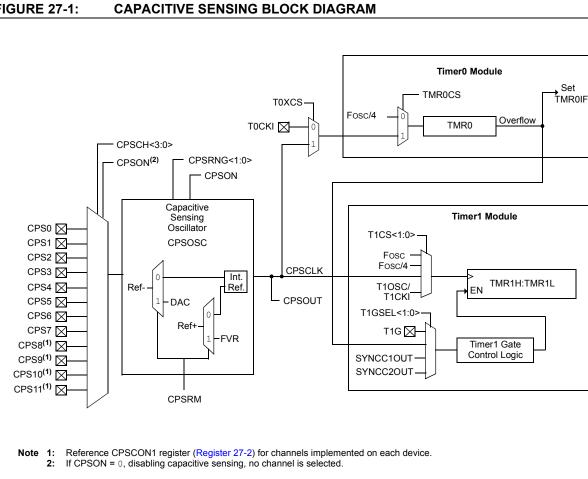
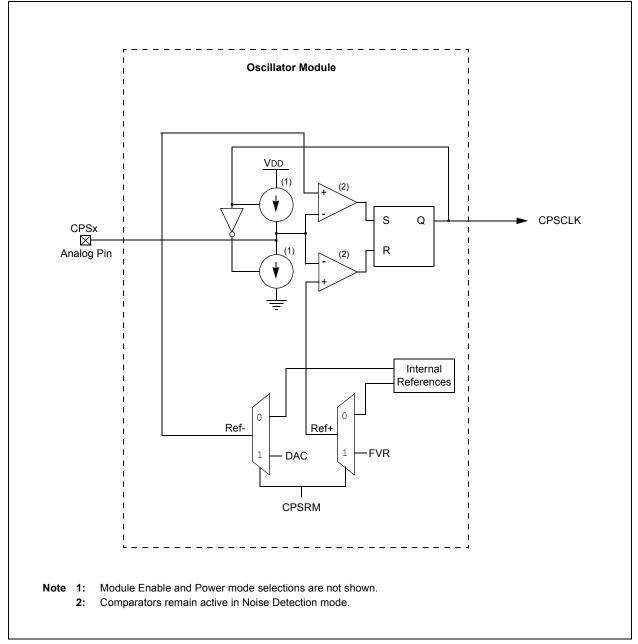


FIGURE 27-1:

FIGURE 27-2: CAPACITIVE SENSING OSCILLATOR BLOCK DIAGRAM



27.1 Analog MUX

The CPS module can monitor up to four inputs for the PIC16F/LF1825 (CPSCH<7:0>) and up to eight inputs for the PIC16F/LF1829 (CPSCH<11:0>). See Register 27-2 for details. The capacitive sensing inputs are defined as CPS<11:0>, as applicable to device. To determine if a frequency change has occurred the user must:

- Select the appropriate CPS pin by setting the CPSCH<3:0> bits of the CPSCON1 register.
- · Set the corresponding ANSEL bit.
- Set the corresponding TRIS bit.
- Run the software algorithm.

The CPS module can monitor up to four inputs for the PIC16F/LF1825 (CPSCH<7:0>) and up to eight inputs for the PIC16F/LF1829 (CPSCH<11:0>). See Register 27-2 for details. The capacitive sensing inputs are defined as CPS<11:0>, as applicable to device. To determine if a frequency change has occurred the user must:

- Select the appropriate CPS pin by setting the appropriate CPSCH bits of the CPSCON1 register.
- Set the corresponding ANSEL bit.
- Set the corresponding TRIS bit.
- Run the software algorithm.

Selection of the CPSx pin while the module is enabled will cause the capacitive sensing oscillator to be on the CPSx pin. Failure to set the corresponding ANSEL and TRIS bits can cause the capacitive sensing oscillator to stop, leading to false frequency readings.

27.2 Capacitive Sensing Oscillator

The capacitive sensing oscillator consists of a constant current source and a constant current sink, to produce a triangle waveform. The CPSOUT bit of the CPSCON0 register shows the status of the capacitive sensing oscillator, whether it is a sinking or sourcing current. The oscillator is designed to drive a capacitive load (single PCB pad) and at the same time, be a clock source to either Timer0 or Timer1. The oscillator has three different current settings as defined by CPSRNG<1:0> of the CPSCON0 register. The different current settings for the oscillator serve two purposes:

- Maximize the number of counts in a timer for a fixed time base.
- Maximize the count differential in the timer during a change in frequency.

27.3 Voltage References

The capacitive sensing oscillator uses voltage references to provide two voltage thresholds for oscillation. The upper voltage threshold is referred to as Ref+ and the lower voltage threshold is referred to as Ref-.

The user can elect to use fixed voltage references, which are internal to the capacitive sensing oscillator, or variable voltage references, which are supplied by the Fixed Voltage Reference (FVR) module and the Digital-to-Analog Converter (DAC) module.

When the fixed voltage references are used, the VSS voltage determines the lower threshold level (Ref-) and the VDD voltage determines the upper threshold level (Ref+).

When the variable voltage references are used, the DAC voltage determines the lower threshold level (Ref-) and the FVR voltage determines the upper threshold level (Ref+). An advantage of using these reference sources is that oscillation frequency remains constant with changes in VDD.

Different oscillation frequencies can be obtained through the use of these variable voltage references. The more the upper voltage reference level is lowered and the more the lower voltage reference level is raised, the higher the capacitive sensing oscillator frequency becomes.

Selection between the voltage references is controlled by the CPSRM bit of the CPSCON0 register. Setting this bit selects the variable voltage references and clearing this bit selects the fixed voltage references.

Please see Section 14.0 "Fixed Voltage Reference (FVR)" and Section 17.0 "Digital-to-Analog Converter (DAC) Module" for more information on configuring the variable voltage levels.

27.4 Power Modes

The capacitive sensing oscillator can operate in one of seven different power modes. The power modes are separated into two ranges; the low range and the high range.

When the oscillator's low range is selected, the fixed internal voltage references of the capacitive sensing oscillator are being used. When the oscillator's high range is selected, the variable voltage references supplied by the FVR and DAC modules are being used. Selection between the voltage references is controlled by the CPSRM bit of the CPSCON0 register. See **Section 27.3** "Voltage References" for more information.

Within each range there are three distinct Power modes; low, medium and high. Current consumption is dependent upon the range and mode selected. Selecting Power modes within each range is accomplished by configuring the CPSRNG <1:0> bits in the CPSCON0 register. See Table 27-1 for proper Power mode selection. The remaining mode is a Noise Detection mode that resides within the high range. The Noise Detection mode is unique in that it disables the sinking and sourcing of current on the analog pin but leaves the rest of the oscillator circuitry active. This reduces the oscillation frequency on the analog pin to zero and also greatly reduces the current consumed by the oscillator module.

When noise is introduced onto the pin, the oscillator is driven at the frequency determined by the noise. This produces a detectable signal at the comparator output, indicating the presence of activity on the pin.

Figure 27-2 shows a more detailed drawing of the current sources and comparators associated with the oscillator.

CPSRM	Range	CPSRNG<1:0>	Mode Nominal Current ⁽	
	00 Of		Off	0.0 μA
0	Low	01	Low	0.1 μA
0	Low	10	Medium	1.2 μA
		11	High	18 μA
		00	Noise Detection	0.0 μA
1	High	01 Low		9 μA
	High	10	Medium 30 μ	
		11	High	100 μA

TABLE 27-1: POWER MODE SELECTION

Note 1: See Section 30.0 "Electrical Specifications" for more information.

27.5 Timer Resources

To measure the change in frequency of the capacitive sensing oscillator, a fixed time base is required. For the period of the fixed time base, the capacitive sensing oscillator is used to clock either Timer0 or Timer1. The frequency of the capacitive sensing oscillator is equal to the number of counts in the timer divided by the period of the fixed time base.

27.6 Fixed Time Base

To measure the frequency of the capacitive sensing oscillator, a fixed time base is required. Any timer resource or software loop can be used to establish the fixed time base. It is up to the end user to determine the method in which the fixed time base is generated.

Note:	The fixed time base can not be generated
	by the timer resource that the capacitive
	sensing oscillator is clocking.

27.6.1 TIMER0

To select Timer0 as the timer resource for the CPS module:

- Set the T0XCS bit of the CPSCON0 register.
- Clear the TMR0CS bit of the OPTION register.

When Timer0 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer0. Refer to **Section 20.0** "**Timer0 Module**" for additional information.

27.6.2 TIMER1

To select Timer1 as the timer resource for the CPS module, set the TMR1CS<1:0> of the T1CON register to '11'. When Timer1 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer1. Because the Timer1 module has a gate control, developing a time base for the frequency measurement can be simplified by using the Timer0 overflow flag.

It is recommend that the Timer0 overflow flag, in conjunction with the Toggle mode of the Timer1 Gate, be used to develop the fixed time base required by the software portion of the CPS module. Refer to **Section 21.12 "Timer1 Gate Control Register"** for additional information.

TMR10N	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	On
1	1	Count Enabled by input

27.7 Software Control

The software portion of the CPS module is required to determine the change in frequency of the capacitive sensing oscillator. This is accomplished by the following:

- Setting a fixed time base to acquire counts on Timer0 or Timer1.
- Establishing the nominal frequency for the capacitive sensing oscillator.
- Establishing the reduced frequency for the capacitive sensing oscillator due to an additional capacitive load.
- Set the frequency threshold.

27.7.1 NOMINAL FREQUENCY (NO CAPACITIVE LOAD)

To determine the nominal frequency of the capacitive sensing oscillator:

- Remove any extra capacitive load on the selected CPSx pin.
- At the start of the fixed time base, clear the timer resource.
- At the end of the fixed time base save the value in the timer resource.

The value of the timer resource is the number of oscillations of the capacitive sensing oscillator for the given time base. The frequency of the capacitive sensing oscillator is equal to the number of counts on in the timer divided by the period of the fixed time base.

27.7.2 REDUCED FREQUENCY (ADDITIONAL CAPACITIVE LOAD)

The extra capacitive load will cause the frequency of the capacitive sensing oscillator to decrease. To determine the reduced frequency of the capacitive sensing oscillator:

- Add a typical capacitive load on the selected CPSx pin.
- Use the same fixed time base as the nominal frequency measurement.
- At the start of the fixed time base, clear the timer resource.
- At the end of the fixed time base save the value in the timer resource.

The value of the timer resource is the number of oscillations of the capacitive sensing oscillator with an additional capacitive load. The frequency of the capacitive sensing oscillator is equal to the number of counts on in the timer divided by the period of the fixed time base. This frequency should be less than the value obtained during the nominal frequency measurement.

27.7.3 FREQUENCY THRESHOLD

The frequency threshold should be placed midway between the value of nominal frequency and the reduced frequency of the capacitive sensing oscillator. Refer to Application Note AN1103, "*Software Handling for Capacitive Sensing*" (DS01103) for more detailed information on the software required for CPS module.

Note:	For more information on general capacitive sensing refer to Application Notes:
	 AN1101, "Introduction to Capacitive Sensing" (DS01101)
	 AN1102, "Layout and Physical Design Guidelines for Capacitive

Sensing" (DS01102)

27.8 Operation during Sleep

The capacitive sensing oscillator will continue to run as long as the module is enabled, independent of the part being in Sleep. In order for the software to determine if a frequency change has occurred, the part must be awake. However, the part does not have to be awake when the timer resource is acquiring counts.

Note: Timer0 does not operate when in Sleep, and therefore cannot be used for capacitive sense measurements in Sleep.

R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R-0/0	R/W-0/0
CPSON	CPSRM	—	—	CPSRI	NG<1:0>	CPSOUT	TOXCS
bit 7							bit (
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkr				R/Value at all o	ther Resets
'1' = Bit is set	•	'0' = Bit is clea	ared				
bit 7	1 = CPS mo	S Module Enabl dule is enabled dule is disabled					
bit 6	1 = CPS mo		ange. DAC a	Mode bit ind FVR provide rnal oscillator ve			
bit 5-4	Unimplemen	ted: Read as ')'				
bit 3-2	<u>If CPSRM = 0</u> 00 = Oscillate 01 = Oscillate 10 = Oscillate	or is in Low Rar or is in Medium	nge. Charge/ Range. Cha	Discharge Curre rge/Discharge Curre /Discharge Curr	Current is nomi	nally 1.2 μA	
	00 = Oscillate 01 = Oscillate 10 = Oscillate	or is in Low Rar or is in Medium	nge. Charge/ Range. Cha	ode. No Charge/ Discharge Curre rge/Discharge C /Discharge Curr	ent is nominally Current is nomi	/ 9 μΑ nally 30 μΑ	
bit 1	CPSOUT: Capacitive Sensing Oscillator Status bit 1 = Oscillator is sourcing current (Current flowing out of the pin) 0 = Oscillator is sinking current (Current flowing into the pin)						
bit 0	If TMR0CS = The T0XCS b 1 = Timer0 0 = Timer0 If TMR0CS =	bit controls whic clock source is clock source is 0:	h clock exter the capacitiv the T0CKI pi	rnal to the core/ e sensing oscill	ator		0:

REGISTER 27-1: CPSCON0: CAPACITIVE SENSING CONTROL REGISTER 0

U-0	U-0	U-0	U-0	R/W-0/0 ⁽¹⁾	R/W-0/0	R/W-0/0	R/W-0/0
_	—	—	_	CPSCI	H<3:2>	CPSC	H<1:0>
bit 7							bit
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpleme	ented bit, read a	as 'O'	
u = Bit is unch	anged	x = Bit is unkno	own	-n/n = Value at	POR and BOR	/Value at all oth	er Resets
'1' = Bit is set		'0' = Bit is clea	red				
bit 7-4	Unimplement	ted: Read as '0'					
bit 3-0	CPSCH<3:0>	: Capacitive Sen	ising Channe	I Select bits			
	<u>If CPSON = 0</u>	:					
		ts are ignored. N	o channel is	selected.			
	<u>If CPSON = 1</u> :						
		channel 0, (CPS	,				
		channel 1, (CPS	,				
		channel 2, (CPS	,				
		channel 3, (CPS	,				
		channel 4, (CPS					
		channel 5, (CPS					
		channel 6, (CPS channel 7, (CPS					
		channel 8, (CPS					
		channel 9, (CPS					
	1001 -	channel 10, (CF	(1) = (1)				
		channel 11, (CF					
		Reserved. Do n					
	•		101 430.				
	•						
	•						
	1111 =	Reserved. Do n	otuso				

REGISTER 27-2: CPSCON1: CAPACITIVE SENSING CONTROL REGISTER 1

Note 1: These channels are only implemented on the PIC16F/LF1829.

	TABLE 27-3:	SUMMARY OF REGISTERS ASSOCIATED WITH CAPACITIVE SENSING
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Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	_	_	ANSA4	_	ANSA2	ANSA1	ANSA0	130
ANSELC	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	_	_	ANSC3	ANSC2	ANSC1	ANSC0	141
CPSCON0	CPSON	CPSRM	_	_	CPSRNG1	CPSRNG0	CPSOUT	T0XCS	333
CPSCON1	—	_	_	_	CPSCH3	CPSCH2	CPSCH1	CPSCH0	334
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	131
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	_	_	_	_	136
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	142
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	93
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA	PS2	PS1	PS0	189
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	—	TMR10N	199
TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	129
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	—	—	_	—	135
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	140

Legend: — = Unimplemented locations, read as '0'. Shaded cells are not used by the CPS module. Note 1: PIC16F/LF1829 only.

28.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP[™] programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP[™] programming:

- ICSPCLK
- ICSPDAT
- MCLR/VPP
- VDD
- Vss

In Program/Verify mode the Program Memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the "*PIC16F/LF182X/PIC12F/LF1822 Memory Programming Specification*" (DS41403).

28.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on MCLR/VPP to VIHH.

Some programmers produce VPP greater than VIHH (9.0V), an external circuit is required to limit the VPP voltage. See Figure 28-1 for example circuit.

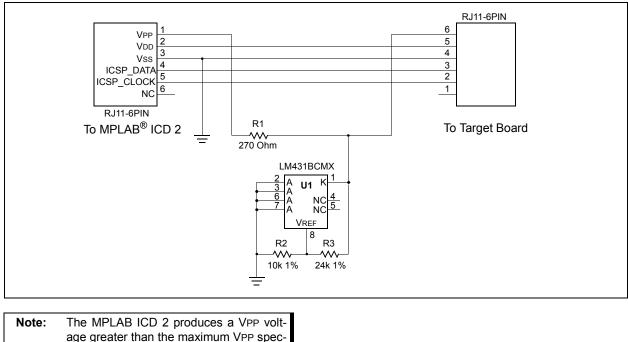


FIGURE 28-1: VPP LIMITER EXAMPLE CIRCUIT

ification of the PIC16F/LF1825/1829.

28.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC16F/LF1825/1829 devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

- 1. $\overline{\text{MCLR}}$ is brought to VIL.
- 2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

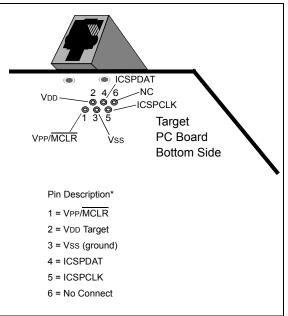
If low-voltage programming is enabled (LVP = 1), the $\overline{\text{MCLR}}$ Reset function is automatically enabled and cannot be disabled. See **Section 7.3 "MCLR**" for more information.

The LVP bit can only be reprogrammed to '0' by using the High-Voltage Programming mode.

28.3 Common Programming Interfaces

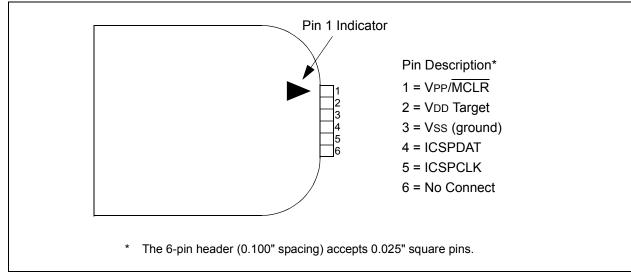
Connection to a target device is typically done through an ICSP[™] header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6 pin, 6 connector) configuration. See Figure 28-2.

FIGURE 28-2: ICD RJ-11 STYLE CONNECTOR INTERFACE



Another connector often found in use with the PICkit[™] programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 28-3.

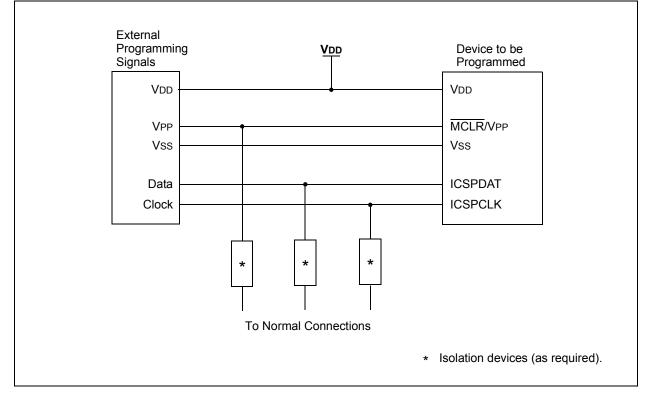
FIGURE 28-3: PICkit[™] STYLE CONNECTOR INTERFACE



For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 28-4 for more information.





NOTES:

29.0 INSTRUCTION SET SUMMARY

Each PIC16 instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories.

- Byte Oriented
- · Bit Oriented
- Literal and Control

The literal and control category contains the most varied instruction word format.

Table 29-3 lists the instructions recognized by the MPASMTM assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

29.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

TABLE 29-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0 . It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
n	FSR or INDF number. (0-1)
mm	Pre-post increment-decrement mode selection

TABLE 29-2: ABBREVIATION DESCRIPTIONS

Field	Description
PC	Program Counter
TO	Time-out bit
С	Carry bit
DC	Digit carry bit
Z	Zero bit
PD	Power-down bit

FIGURE 29-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations 13 8 7 6 0
13 8 7 6 0 OPCODE d f(FILE #)
d = 0 for destination W d = 1 for destination f f = 7-bit file register address
Bit-oriented file register operations
OPCODE b (BIT #) f (FILE #)
b = 3-bit bit address f = 7-bit file register address
Literal and control operations
General
13 8 7 0 OPCODE k (literal)
k = 8-bit immediate value
CALL and GOTO instructions only
13 11 10 0
OPCODE k (literal)
k = 11-bit immediate value
MOVLP instruction only 13 7 6 0
OPCODE k (literal)
k = 7-bit immediate value
MOVLB instruction only
13 5 4 0
OPCODE k (literal)
k = 5-bit immediate value
BRA instruction only
13 9 8 0 OPCODE k (literal)
k = 9-bit immediate value
FSR Offset instructions
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
OPCODE n k (literal)
n = appropriate FSR k = 6-bit immediate value
FSR Increment instructions 13
OPCODE n m (mode)
n = appropriate FSR m = 2-bit mode value
OPCODE only 13 0
OPCODE

Mnemonic, Operands		Description Cycles -		14-Bit Opcode				Status	Notes
				MSb			LSb	Affected	Note
		BYTE-ORIENTED FILE	E REGISTER OPE	RATIO	NS				
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	2
ADDWFC	f, d	Add with Carry W and f	1	11	1101	dfff	ffff	C, DC, Z	2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	2
ASRF	f, d	Arithmetic Right Shift	1	11	0111	dfff	ffff	C, Z	2
LSLF	f, d	Logical Left Shift	1	11	0101	dfff	ffff	C, Z	2
LSRF	f, d	Logical Right Shift	1	11	0110	dfff	ffff	C, Z	2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	_	Clear W	1	00	0001	0000	00xx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	2
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	2
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		2
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	2
SUBWF	f. d	Subtract W from f	1	00	0010		ffff	C, DC, Z	2
SUBWFB	f, d	Subtract with Borrow W from f	1	11	1011		ffff	C, DC, Z	2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff		-,, -	2
XORWF	f, d	Exclusive OR W with f	1	00	0110		ffff	Z	2
		BYTE ORIENTEI		ONS					
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1, 2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1, 2
		BIT-ORIENTED FILE	REGISTER OPER	RATION	IS				
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		2
		BIT-ORIENTED	SKIP OPERATIO	NS					
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		1, 2
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		1, 2
LITERAL	OPERA	TIONS	·						
ADDLW	k	Add literal and W	1	11	1110	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLB	k	Move literal to BSR	1	00	0000	001k	kkkk		
MOVLP	k	Move literal to PCLATH	1	11	0001	1kkk	kkkk		
MOVLW	k	Move literal to W	1	11	0000	kkkk	kkkk		
SUBLW	k	Subtract W from literal	1	11	1100	kkkk	kkkk	C, DC, Z	
COBLII									

TABLE 29-3: PIC16F/LF1825/1829 ENHANCED INSTRUCTION SET

Note 1: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

Mnemonic, Operands		Description	Cycles	14-Bit Opcode			Status	Notes	
		Description	Cycles	MSb			LSb	Affected	Notes
		CONTROL OPERA	TIONS						
BRA	k	Relative Branch	2	11	001k	kkkk	kkkk		
BRW	-	Relative Branch with W	2	00	0000	0000	1011		
CALL	k	Call Subroutine	2	10	0 k k k	kkkk	kkkk		
CALLW	-	Call Subroutine with W	2	00	0000	0000	1010		
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
RETFIE	k	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	0100	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
		INHERENT OPERA	TIONS						
CLRWDT	_	Clear Watchdog Timer	1	00	0000	0110	0100	TO, PD	
NOP	-	No Operation	1	00	0000	0000	0000		
OPTION	-	Load OPTION_REG register with W	1	00	0000	0110	0010		
RESET	-	Software device Reset	1	00	0000	0000	0001		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO, PD	
TRIS	f	Load TRIS register with W	1	00	0000	0110	Offf		
		C-COMPILER OPT	IMIZED						
ADDFSR	n, k	Add Literal k to FSRn	1	11	0001	0nkk	kkkk		
MOVIW	n mm	Move Indirect FSRn to W with pre/post inc/dec	1	00	0000	0001	0nmm	Z	2, 3
		modifier, mm					kkkk		
	k[n]	Move INDFn to W, Indexed Indirect.	1	11	1111	Onkk	1nmm	Z	2
MOVWI	n mm	Move W to Indirect FSRn with pre/post inc/dec	1	00	0000	0001	kkkk		2, 3
		modifier, mm							
	k[n]	Move W to INDFn, Indexed Indirect.	1	11	1111	1nkk			2

TABLE 29-3: PIC16F/LF1825/1829 ENHANCED INSTRUCTION SET (CONTINUED)

Note 1: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

3: See Table in the MOVIW and MOVWI instruction descriptions.

Instruction Descriptions 29.2

ADDFSR	Add Literal to FSRn
Syntax:	[label] ADDFSR FSRn, k
Operands:	$-32 \le k \le 31$ n \in [0, 1]
Operation:	$FSR(n) + k \rightarrow FSR(n)$
Status Affected:	None
Description:	The signed 6-bit literal 'k' is added to the contents of the FSRnH:FSRnL register pair.
	ECDs is limited to the second 0000h

FSRn is limited to the range 0000h -FFFFh. Moving beyond these bounds will cause the FSR to wrap around.

ANDLW	AND literal with W		
Syntax:	[<i>label</i>] ANDLW k		
Operands:	$0 \leq k \leq 255$		
Operation:	(W) .AND. (k) \rightarrow (W)		
Status Affected:	Z		
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.		

ADDLW	Add literal and W			
Syntax:	[<i>label</i>] ADDLW k			
Operands:	$0 \leq k \leq 255$			
Operation:	$(W) + k \to (W)$			
Status Affected:	C, DC, Z			
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.			

ANDWF	AND W with f
Syntax:	[<i>label</i>] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) \rightarrow (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ADDWF	Add W and f		
Syntax:	[<i>label</i>] ADDWF f,d		
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$		
Operation:	(W) + (f) \rightarrow (destination)		
Status Affected:	C, DC, Z		
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.		

ASRF	Arithmetic Right Shift
Syntax:	[<i>label</i>]ASRF f{,d}
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	$(f<7>) \rightarrow dest<7>$ $(f<7:1>) \rightarrow dest<6:0>,$ $(f<0>) \rightarrow C,$
Status Affected:	C, Z
Description:	The contents of register 'f' are shifted one bit to the right through the Carry flag. The MSb remains unchanged. If 'd' is '0', the result is placed in W. If 'd'

ister 'f'.

_	_				
	•	register f	→	С	

is '1', the result is stored back in reg-

ADDWFC	ADD W and CARRY bit to f			
Syntax:	[<i>label</i>] ADDWFC f {,d}			
Operands:	$0 \le f \le 127$ $d \in [0,1]$			
Operation:	$(W) + (f) + (C) \rightarrow dest$			
Status Affected:	C, DC, Z			
Description:	Add W, the Carry flag and data mem- ory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'.			

BCF	Bit Clear f
Syntax:	[<i>label</i>]BCF f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	$0 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[label] BTFSC f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	skip if (f) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

BRA	Relative Branch	BT
Syntax:	[<i>label</i>]BRA label [<i>label</i>]BRA \$+k	Syn Ope
Operands:	-256 \leq label - PC + 1 \leq 255 -256 \leq k \leq 255	Ope
Operation:	$(PC) + 1 + k \rightarrow PC$	Stat
Status Affected:	None	Des
Description:	Add the signed 9-bit literal 'k' to the PC. Since the PC will have incre- mented to fetch the next instruction, the new address will be PC + 1 + k. This instruction is a two-cycle instruc- tion. This branch has a limited range.	

BTFSS	Bit Test f, Skip if Set
Syntax:	[<i>label</i>]BTFSS f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b < 7 \end{array}$
Operation:	skip if (f) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

BRW	Relative Branch with W
Syntax:	[label] BRW
Operands:	None
Operation:	$(PC) + (W) \to PC$
Status Affected:	None
Description:	Add the contents of W (unsigned) to the PC. Since the PC will have incre- mented to fetch the next instruction, the new address will be PC + 1 + (W). This instruction is a two-cycle instruc- tion.

BSF	Bit Set f
Syntax:	[<i>label</i>]BSF f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	1 → (f)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

CALL	Call Subroutine
Syntax:	[<i>label</i>] CALL k
Operands:	$0 \leq k \leq 2047$
Operation:	$\begin{array}{l} (PC)+1 \rightarrow TOS, \\ k \rightarrow PC<10:0>, \\ (PCLATH<4:3>) \rightarrow PC<12:11> \end{array}$
Status Affected:	None
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10.0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

CLRWDT	Clear Watchdog Timer
Syntax:	[label] CLRWDT
Operands:	None
Operation:	$00h \rightarrow WDT$ $0 \rightarrow WDT \text{ prescaler,}$ $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$
Status Affected:	TO, PD
Description:	CLRWDT instruction resets the Watch- dog Timer. It also resets the prescaler of the WDT. Status bits \overline{TO} and \overline{PD} are set.

CALLW	Subroutine Call With W	COMF	Complement f
Syntax:	[label] CALLW	Syntax:	[label] COMF
Operands:	None	Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(PC) +1 \rightarrow TOS, (W) \rightarrow PC<7:0>, (PCLATH<6:0>) \rightarrow PC<14:8>	Operation: Status Affected:	$(\bar{f}) \rightarrow (destination)$
Status Affected:	None	Description:	The contents of rep plemented. If 'd' is
Description:	Subroutine call with W. First, the return address (PC + 1) is pushed onto the return stack. Then, the contents of W is loaded into PC<7:0>, and the contents of PCLATH into PC<14:8>. CALLW is a two-cycle instruction.		stored in W. If 'd' is stored back in regi

ax:	[<i>label</i>] COMF f,d
ands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
ation:	$(\overline{f}) \rightarrow (destination)$
s Affected:	Z
ription:	The contents of register 'f' are com- plemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

CLRF	Clear f
Syntax:	[<i>label</i>] CLRF f
Operands:	$0 \leq f \leq 127$
Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

DECF	Decrement f
Syntax:	[<i>label</i>] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 \rightarrow (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} \text{O0h} \rightarrow (\text{W}) \\ 1 \rightarrow \text{Z} \end{array}$
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] DECFSZ f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) - 1 \rightarrow (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decre- mented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \leq k \leq 2047$
Operation:	$k \rightarrow PC<10:0>$ PCLATH<4:3> \rightarrow PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[<i>label</i>] INCFSZ f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incre- mented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

IORLW	Inclusive OR literal with W
Syntax:	[<i>label</i>] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .OR. $k \rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

INCF	Increment f	IORWF	Inclusive OR W with f
Syntax:	[label] INCF f,d	Syntax:	[<i>label</i>] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$	Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (destination)	Operation:	(W) .OR. (f) \rightarrow (destination)
Status Affected:	Z	Status Affected:	Z
Description:	The contents of register 'f' are incre- mented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.	Description:	Inclusive OR the W register with regis- ter 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

LSLF	Logical Left Shift
Syntax:	[<i>label</i>] LSLF f {,d}
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	$(f<7>) \rightarrow C$ $(f<6:0>) \rightarrow dest<7:1>$ $0 \rightarrow dest<0>$
Status Affected:	C, Z
Description:	The contents of register 'f' are shifted one bit to the left through the Carry flag. A '0' is shifted into the LSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.
	C register f -0

LSRF	Logical Right Shift
Syntax:	[<i>label</i>]LSLF f{,d}

Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$
Operation:	$\begin{array}{l} 0 \rightarrow dest < 7 > \\ (f < 7 : 1 >) \rightarrow dest < 6 : 0 >, \\ (f < 0 >) \rightarrow C, \end{array}$
Status Affected:	C, Z
Description:	The contents of register 'f' are shifted one bit to the right through the Carry flag. A '0' is shifted into the MSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.
	0 → register f → C

MOVF	Move f
Syntax:	[<i>label</i>] MOVF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	$(f) \rightarrow (dest)$
Status Affected:	Z
Description:	The contents of register f is moved to a destination dependent upon the status of d. If $d = 0$, destination is W register. If $d = 1$, the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	MOVF FSR, 0
	After Instruction W = value in FSR register Z = 1

ΜΟΥΙΨ	Move INDFn to W
Syntax:	[<i>label</i>] MOVIW ++FSRn [<i>label</i>] MOVIWFSRn [<i>label</i>] MOVIW FSRn++ [<i>label</i>] MOVIW FSRn [<i>label</i>] MOVIW k[FSRn]
Operands:	$n \in [0,1]$ $mm \in [00,01, 10, 11]$ $-32 \le k \le 31$
Operation:	$\begin{split} &\text{INDFn} \rightarrow W \\ &\text{Effective address is determined by} \\ &\text{FSR + 1 (preincrement)} \\ &\text{FSR - 1 (predecrement)} \\ &\text{FSR + k (relative offset)} \\ &\text{After the Move, the FSR value will be} \\ &\text{either:} \\ &\text{FSR + 1 (all increments)} \\ &\text{FSR - 1 (all decrements)} \\ &\text{Unchanged} \end{split}$
Status Affected:	Z

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn	11

Description:

This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h -FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap around.

MOVLB Move literal to BSR

Syntax:	[<i>label</i>]MOVLB k
Operands:	$0 \leq k \leq 15$
Operation:	$k \rightarrow BSR$
Status Affected:	None
Description:	The five-bit literal 'k' is loaded into the Bank Select Register (BSR).

MOVLP	Move literal to PCLATH
Syntax:	[<i>label</i>]MOVLP k
Operands:	$0 \le k \le 127$
Operation:	$k \rightarrow PCLATH$
Status Affected:	None
Description:	The seven-bit literal 'k' is loaded into the PCLATH register.
MOVLW	Move literal to W
Syntax:	[<i>label</i>] MOVLW k
Syntax: Operands:	[<i>label</i>] MOVLW k 0 ≤ k ≤ 255
2	
Operands:	$0 \le k \le 255$
Operands: Operation:	$0 \le k \le 255$ k \rightarrow (W)
Operands: Operation: Status Affected:	$0 \le k \le 255$ $k \to (W)$ None The eight-bit literal 'k' is loaded into W register. The "don't cares" will assem-

MOVLW	02	5A	
After Instru	ctior	n	
V	N	=	0x5A

MOVLW

Example:

MOVWF	Move W to f
Syntax:	[<i>label</i>] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	MOVWF OPTION
	$\begin{array}{rrrr} \text{Before Instruction} & & \\ & \text{OPTION} & = & 0\text{xFF} \\ W & = & 0\text{x4F} \\ \text{After Instruction} & & \\ & \text{OPTION} & = & 0\text{x4F} \\ W & = & 0\text{x4F} \end{array}$

MOVWI	Move W to INDFn
Syntax:	[<i>label</i>] MOVWI ++FSRn [<i>label</i>] MOVWIFSRn [<i>label</i>] MOVWI FSRn++ [<i>label</i>] MOVWI FSRn [<i>label</i>] MOVWI k[FSRn]
Operands:	n ∈ [0,1] mm ∈ [00,01,10,11] -32 ≤ k ≤ 31
Operation:	 W → INDFn Effective address is determined by FSR + 1 (preincrement) FSR - 1 (predecrement) FSR + k (relative offset) After the Move, the FSR value will be either: FSR + 1 (all increments) FSR - 1 (all decrements) Unchanged
Status Affected:	None

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn	11

Description:

This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h -FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap around.

The increment/decrement operation on FSRn WILL NOT affect any Status bits.

NOP **No Operation** Syntax: [label] NOP Operands: None Operation: No operation Status Affected: None Description: No operation. Words: 1 Cycles: 1

NOP

Example:

OPTION	Load OPTION_REG Register with W
Syntax:	[label] OPTION
Operands:	None
Operation:	$(W) \to OPTION_REG$
Status Affected:	None
Description:	Move data from W register to OPTION_REG register.

RESET	Software Reset
Syntax:	[<i>label</i>] RESET
Operands:	None
Operation:	Execute a device Reset. Resets the nRI flag of the PCON register.
Status Affected:	None
Description:	This instruction provides a way to execute a hardware Reset by software.

RETFIE	Return from Interrupt
Syntax:	[label] RETFIE
Operands:	None
Operation:	$TOS \rightarrow PC, \\ 1 \rightarrow GIE$
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
Example:	RETFIE
	After Interrupt PC = TOS GIE = 1

RETURN	Return from Subroutine		
Syntax:	[label] RETURN		
Operands:	None		
Operation:	$TOS \rightarrow PC$		
Status Affected:	None		
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.		

RETLW	Return with literal in W	RLF	Rotate Left f through Carry
Syntax:	[<i>label</i>] RETLW k	Syntax:	[<i>label</i>] RLF f,d
Operands:	$0 \leq k \leq 255$	Operands:	$0 \leq f \leq 127$
Operation:	$k \rightarrow (W);$ TOS \rightarrow PC	Operation:	$d \in [0,1]$ See description below
Status Affected:	None	Status Affected:	С
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.	Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.
Words:	1		C Register f
Cycles: <u>Example:</u>	2 CALL TABLE;W contains table	Words:	1
; offset value • ;W now has table value		Cycles: <u>Example:</u>	1 RLF REG1,0
TABLE	•		Before Instruction REG1 = 1110 0110
	ADDWF PC ;W = offset RETLW k1 ;Begin table		C = 0 After Instruction
	RETLW k2 ; •		REG1 = 1110 0110 W = 1100 1100
	•		C = 1
	RETLW kn ; End of table		
	Before Instruction W = 0x07 After Instruction W = value of k8		

RRF	Rotate Right f through Carry	
Syntax:	[<i>label</i>] RRF f,d	
Operands:	$0 \le f \le 127$ $d \in [0,1]$	
Operation:	See description below	
Status Affected:	С	
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.	
	C Register f	

SUBLW	Subtract W from literal		
Syntax:	[label] Sl	JBLW k	
Operands:	$0 \le k \le 255$		
Operation:	$k - (W) \rightarrow (W)$		
Status Affected:	C, DC, Z		
Description:	The W register is subtracted (2's com- plement method) from the eight-bit literal 'k'. The result is placed in the W register.		
	C = 0	W > k	
	C = 1	$W \le k$	
	DC = 0	W<3:0> > k<3:0>	

DC = 1

 $W<3:0> \le k<3:0>$

 $W<3:0> \le f<3:0>$

SLEEP	Enter Sleep mode
Syntax:	[label] SLEEP
Operands:	None
Operation:	$\begin{array}{l} \text{O0h} \rightarrow \text{WDT,} \\ 0 \rightarrow \text{WDT prescaler,} \\ 1 \rightarrow \overline{\text{TO}}, \\ 0 \rightarrow \overline{\text{PD}} \end{array}$
Status Affected:	TO, PD
Description:	The power-down Status bit, $\overline{\text{PD}}$ is cleared. Time-out Status bit, $\overline{\text{TO}}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBWF	Subtract W	/ from f						
Syntax:	[label] SL	JBWF f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$							
Operation:	(f) - (W) → (d)	lestination)						
Status Affected:	C, DC, Z							
Description:	register from result is store	is '1', the result is stored						
	C = 0	C = 0 W > f						
	C = 1	$W \leq f$						
	DC = 0	W<3:0> > f<3:0>						

SUBWFB	Subtract W from f with Borrow
Syntax:	SUBWFB f {,d}
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(f) - (W) - (\overline{B}) \rightarrow dest$
Status Affected:	C, DC, Z
Description:	Subtract W and the BORROW flag (CARRY) from register 'f' (2's comple- ment method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

DC = 1

SWAPF	Swap Nibbles in f
Syntax:	[label] SWAPF f,d
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$
Operation:	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of regis- ter 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW	Exclusive OR literal with W							
Syntax:	[<i>label</i>] XORLW k							
Operands:	$0 \leq k \leq 255$							
Operation:	(W) .XOR. $k \rightarrow (W)$							
Status Affected:	Z							
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.							

TRIS	Load TRIS Register with W	XORWF	Exclusive OR W with f	
Syntax:	[<i>label</i>] TRIS f	Syntax:	[<i>label</i>] XORWF f,d	
Operands:	$5 \le f \le 7$	Operands:	$0 \le f \le 127$	
Operation:	(W) \rightarrow TRIS register 'f'		d ∈ [0,1]	
Status Affected:	None	Operation:	(W) .XOR. (f) \rightarrow (destination)	
Description:	Move data from W register to TRIS	Status Affected:	Z	
	register. When 'f' = 5, TRISA is loaded. When 'f' = 6, TRISB is loaded. When 'f' = 7, TRISC is loaded.	Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.	

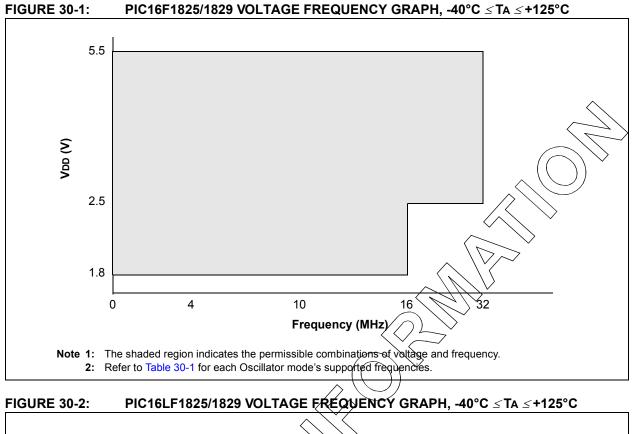
30.0 ELECTRICAL SPECIFICATIONS

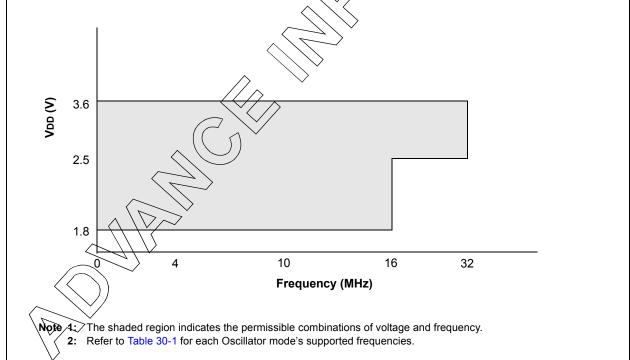
Absolute Maximum Ratings^(†)

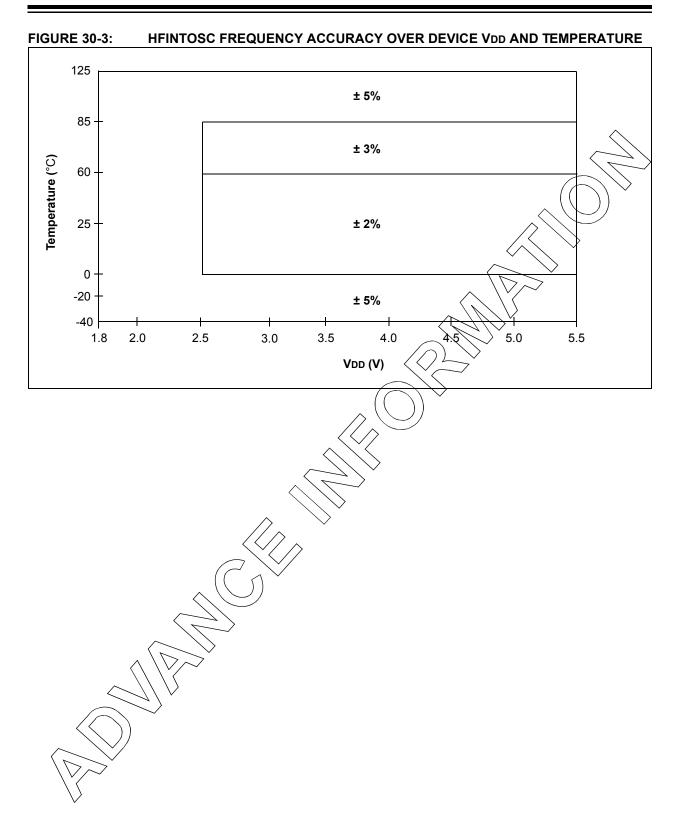
Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss, PIC16F1825/1829	0.3V to +6.5V
Voltage on VDD with respect to Vss, PIC16LF1825/1829	0.3V to +4.0V
Voltage on MCLR with respect to Vss	0.3∀to+9.0V
Voltage on all other pins with respect to Vss	
Total power dissipation ⁽¹⁾	
Maximum current out of Vss pin, -40°C \leq Ta \leq +85°C for industrial	
Maximum current out of Vss pin, -40°C \leq Ta \leq +125°C for extended	
Maximum current into VDD pin, -40°C \leq TA \leq +85°C for industrial	
Maximum current into VDD pin, $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended	
Clamp current, IK (VPIN < 0 or VPIN > VDD)	± 20 mA
Maximum output current sunk by any I/O pin	
Maximum output current sourced by any I/O pin	.)25 mA
Note 1: Power dissipation is calculated as follows: PDIS = VDD x { $IDD - \sum IO$	$\widetilde{H} + \Sigma \{ (VDD - VOH) \times IOH \} + \Sigma (VOI \times IOL). \}$

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

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30.1 DC Characteristics: PIC16F/LF1825/1829-I/E (Industrial, Extended)

PIC16LF	-1825/1829		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq T_A \leq +85^\circ C \mbox{ for industrial} \\ -40^\circ C \leq T_A \leq +125^\circ C \mbox{ for extended} \end{array}$					
PIC16F1	825/1829	_	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param. No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions	
D001	Vdd	Supply Voltage						
		PIC16LF1825/1829	1.8 2.3		3.6 3.6	V V	Fosc ≤ 16 MHz; Fosc ≤ 32 MHz (NOTE 2)	
D001		PIC16F1825/1829	1.8 2.3	_	5.5 5.5	V V	$\begin{array}{l} Fosc \leq 16 \text{ MHz:} \\ Fosc \leq 32 \text{ MHz} (NOTE 2) \end{array}$	
D002*	Vdr	RAM Data Retention Voltage ⁽¹⁾				•	\sim	
		PIC16LF1825/1829	1.5	—	—	V	Device in Sleep mode	
D002*		PIC16F1825/1829	1.7			V <	Device in Sleep mode	
	VPOR*	Power-on Reset Release Voltage		1.6	—	X		
	VPORR*	Power-on Reset Rearm Voltage					\bigtriangledown	
		PIC16LF1825/1829		0.8	_/		Device in Sleep mode	
		PIC16F1825/1829		1.7		\sim	Device in Sleep mode	
D003	VADFVR	Fixed Voltage Reference Voltage for ADC, Initial Accuracy	-7 -8 -7 -8 -7		6 6 6 6 6 6 6		$\begin{array}{l} 1.024V, V_{DD} \geq 2.5V, 85^{\circ}C \mbox{ (NOTE 3)} \\ 1.024V, V_{DD} \geq 2.5V, 125^{\circ}C \mbox{ (NOTE 3)} \\ 2.048V, V_{DD} \geq 2.5V, 85^{\circ}C \\ 2.048V, V_{DD} \geq 2.5V, 125^{\circ}C \\ 4.096V, V_{DD} \geq 4.75V, 85^{\circ}C \\ 4.096V, V_{DD} \geq 4.75V, 125^{\circ}C \end{array}$	
D003A	VCDAFVR	Fixed Voltage Reference Voltage for Comparator and DAC, Initial Accu- racy	++ ++ ++ ++ ++ ++ ++ ++ ++ ++ ++ ++ ++		7 7 7 7 7 7	%	1.024V, $V_{DD} \ge 2.5V$, $85^{\circ}C$ 1.024V, $V_{DD} \ge 2.5V$, $125^{\circ}C$ 2.048V, $V_{DD} \ge 2.5V$, $85^{\circ}C$ 2.048V, $V_{DD} \ge 2.5V$, $125^{\circ}C$ 4.096V, $V_{DD} \ge 4.75V$, $85^{\circ}C$ 4.096V, $V_{DD} \ge 4.75V$, $125^{\circ}C$	
D003C*	TCVFVR	Temperature Coefficient, Fixed Voltage Reference	—	-130	—	ppm/°C		
D003D*	$\Delta VFVR/$ ΔVIN	Line Regulation, Fixed Voltage Reference	—	0.270	—	%/V		
D004*	SVDD	Vod Rise Rate to ensure internal Power-on Reset signal	0.05	—		V/ms	See Section 7.1 "Power-on Reset (POR)" for details.	

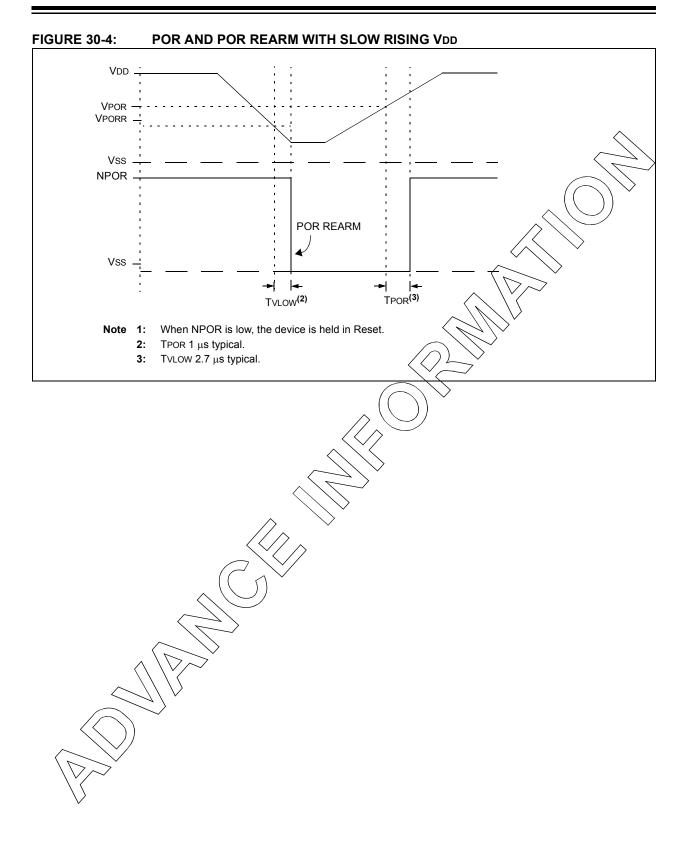
* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: PLL required for 32 MHz operation.

3: For proper operation, the minimum value of the ADC positive voltage reference must be 1.8V or greater. When selecting the FVR or the VREF+ pin as the source of the ADC positive voltage reference, be aware that the voltage must be 1.8V or greater.



30.2 DC Characteristics: PIC16F/LF1825/1829-I/E (Industrial, Extended)

PIC16LF1	825/1829					ess otherwise stated) ≤ +85°C for industrial ≤ +125°C for extended		
PIC16F1825/1829			Standard Operating		iture -	40°C ≤ TA	ess otherwise stated) ≤ +85°C for industrial ≤ +125°C for extended	
Param	Device	Min.	Тур†	Max.	Units		Conditions	
No.	Characteristics					VDD	Note	
	Supply Current (IDD) ^{(1, 2}	2)						
D010			7.0	—	μA	1.8	Fosc = 32 kHz	
		—	9.0	_	μA	3.0	LP Oscillator mode	
D010		—	29	_	μA	1.8	Fosc = 32 kHz	
		—	35	_	μA	3.0	LP Oscillator mode	
		-	38	_	μA	5.0		
D011			110	_	μA	1.8	Fosc = MHz	
			220	_	μA	3.0	XT QsotHator mode	
D011		-	105	_	μA	1.8	Pose = 1 MHz	
			170		μA	30	XT Oscillator mode	
			225		μΑ (5.0	\sim	
D012		—	290	_	μA	1.8	Fosc = 4 MHz	
		—	520	_	$\langle \mathbf{M} \rangle$	3.0	XT Oscillator mode	
D012		_	300	_ <) AU	1.8	Fosc = 4 MHz	
		-	500	$\left\{ \cdot \right\}$	Sur V	3.0	XT Oscillator mode	
		_	600	$\langle - \rangle$	μÂ	5.0		
D013			80	X	ΨµA	1.8	Fosc = 1 MHz	
		_	130	_~	μA	3.0	EC Oscillator mode, Medium-power mode	
D013		_	<100/	\sim	μA	1.8	Fosc = 1 MHz	
		70	7 150	_	μA	3.0	EC Oscillator mode Medium-power mode	
		. +(5190	_	μA	5.0	medium-power mode	
D014	<	$\left< - \right>$	260	_	μA	1.8	Fosc = 4 MHz	
		$ \rightarrow $	450	—	μA	3.0	EC Oscillator mode, Medium-power mode	
D014		\searrow	280	—	μA	1.8	Fosc = 4 MHz	
	$\wedge \langle \nabla \rangle$	7 _	480	_	μA	3.0	EC Oscillator mode Medium-power mode	
	$\sim 1/15$	_	560	_	μA	5.0		

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

- **3:** 8 MHz internal RC oscillator with 4x PLL enabled.
- 4: 8 MHz crystal oscillator with 4x PLL enabled.

5: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

30.2 DC Characteristics: PIC16F/LF1825/1829-I/E (Industrial, Extended) (Continued)

PIC16LF1825/1829							ess otherwise stated) ≤ +85°C for industrial ≤ +125°C for extended
PIC16F1825/1829							ess otherwise stated) $\leq +85^{\circ}$ C for industrial $\leq +125^{\circ}$ C for extended
Param No.	Device Characteristics	Min.	Тур†	Max.	Units	N=-	Conditions
-		2)				VDD	Note
D015	Supply Current (IDD) ^{(1, 7}	<u>-</u>)	3.6			1.8	Fosc = 31 kHz
D015		_	4.0		μA A	3.0	LFINTOSC mode
D015			26		μA μA	1.8	Fosc = 31 kHz
DOID			33		μΑ	3.0	LFINTOSC mode
			35		μΑ	5.0	
D016			110		μA	1.8	Fosc = 500 kHz
		_	150		μA	3.0	MFINIOSC mode
D016		_	120	_	μA	1.8	FQSC = 500 KHz
		_	160	_	μA	3.0 <	MEINTOSC mode
		_	190		μA	5.0	
D017*			0.8	_	mA (1.8	Fosc = 8 MHz
			1.3	_	mA>	3.0	HFINTOSC mode
D017*			0.8	_	(mA/)	1.8	Fosc = 8 MHz
			1.3	_ <	/ mA	3.0	HFINTOSC mode
		—	1.4	$\left\{ \cdot \right\}$	Am	5.0	
D018		—	1.2	$\langle - \rangle$	mĂ	1.8	Fosc = 16 MHz HFINTOSC mode
		_	2.0	\rightarrow	∼mA	3.0	
D018		—	<u>/</u> 2	—	mA	1.8	Fosc = 16 MHz HFINTOSC mode
		-	2.0	/-	mA	3.0	
Data		-10	2.3	(—	mA	5.0	Face OO MUL
D019		$\frac{1}{2}$	<u>(</u> 4)0	—	mA	3.0	Fosc = 32 MHz HFINTOSC mode (Note 3)
D010		X	4.4	—	mA	3.6	· · ·
D019	7	\rightarrow	3.9	—	mA	3.0	Fosc = 32 MHz HFINTOSC mode (Note 3)
	\sim	\searrow	4.2	—	mA	5.0	(

* These parameters are characterized but not tested.

+ Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested

Note 1: The test condition's for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: /8.MHz internal RC oscillator with 4x PLL enabled.

4: \langle 8 MHz crystal oscillator with 4x PLL enabled.

For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in k Ω .

30.2 DC Characteristics: PIC16F/LF1825/1829-I/E (Industrial, Extended) (Continued)

PIC16LF	1825/1829	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
PIC16F18	325/1829			Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param	Device	Min.	Treat	Max.	Units		Conditions		
No.	Characteristics	WIIII.	Тур†	WidX.	Units	Vdd	Note		
	Supply Current (IDD) ^(1,)	2)							
D020		_	3.3	—	mA	3.0	Fosc = 32 MHz		
		_	3.6	_	mA	3.6	HS Oscillator mode (Note 4)		
D020		_	3.3	_	mA	3.0	Fosc = 32 MHz		
		_	3.8	_	mA	5.0	HS Oscillator mode (Note 4)		
D021		_	410	_	μA	1.8	Fosc = 4 MHz		
		_	710	—	μA	3.0	EXTRE mode (Note 5)		
D021		_	430		μA	1.8	Fosc = 4MHz		
		_	730		μA	3.0	EXTRO mode (Note 5)		
		_	860	_	μA	5.0 <			

* These parameters are characterized but not tested.

+ Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDP; WDT disabled.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
- 3: 8 MHz internal RC oscillator with 4x PLL enabled
- 4: 8 MHz crystal oscillator with 4x PLL enabled.
- 5: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ..

DS41440A-page 360

30.3 DC Characteristics: PIC16F/LF1825/1829-I/E (Power-Down)

PIC16LF1825/1829				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for industrial} \\ -40^\circ C \leq TA \leq +125^\circ C \mbox{ for extended} \end{array}$					
PIC16F1825/1829				Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param	Device Characteristics	Min.	Tunt	Max.	Max.	Units		Conditions	
No.	Device Characteristics	wiin.	Тур†	+85°C	+125°C	Units	Vdd	Note	
	Power-down Base Current	(IPD) ⁽²⁾							
D022		_	0.02	—	—	μΑ	1.8	WDT, BOR, FVR, and T1OSC	
		_	0.03	—	_	μA	3.0	disabled, all Peripherals Inactive	
D022		_	19	—	—	μA	1.8	WDT, BOR, FVR, and T1OSC	
		—	23	—	—	μA	3.0	disabled, all Peripherals Inactive	
		—	24	—	—	μA	5,0		
D023		—	0.5	—	—	μA	1.8	LPWDT Current (Note 1)	
		_	0.8	_	_	μA	30	×	
D023		_	1.9	—	_	ШĂ	1.8	LPWDT Current (Note 1)	
		_	2.3	_	—	<ua <="" td=""><td>3.0</td><td></td></ua>	3.0		
		—	2.4	—		Ay	5.0		
D023A		—	8.5	—	+(μĄ	1.8	FVR current (Note 1)	
		_	8.5			lux	3.0		
D023A		_	32	$-\langle$	V7	μA	1.8	FVR current (Note 1)	
		_	38	$ \leftarrow $	\rightarrow	μA	3.0		
D 00 4		_	68	\frown	\rightarrow^{-}	mA	5.0		
D024			8.1	$\overline{/}$	~ _	μA	3.0	BOR Current (Note 1)	
D024		_	30	\searrow	_	μA	3.0	BOR Current (Note 1)	
DOOL		/	> 33	<u>×</u>	—	μA	5.0	T1000 Ourrent (Note 4)	
D025		<u> </u>	0.8	_	_	μA	1.8	T1OSC Current (Note 1)	
DODE	/	$\overline{\Box}$	21			μA	3.0	T1050 Current (Note 1)	
D025		$\left(- \right)$	21			μΑ	1.8 3.0	T1OSC Current (Note 1)	
		Į	24			μΑ μΑ	5.0		
D026		\geq	0.1	_		μΑ	1.8	A/D Current (Note 1, Note 3) , no conversion in progress	
2020		~ _	0.1			μΑ	3.0		
D026		_	16			μΑ	1.8	A/D Current (Note 1, Note 3), no	
2020			21			μΑ	3.0	conversion in progress	
$\sim // \vee$		21			μΑ	5.0			

These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is → enabled. The peripheral △ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2 → The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: A/D oscillator source is FRC.

Note

30.3 DC Characteristics: PIC16F/LF1825/1829-I/E (Power-Down) (Continued)

PIC16LF1825/1829				$\begin{array}{llllllllllllllllllllllllllllllllllll$						
PIC16F1825/1829			Standard Operating Cond Operating temperature			litions (unless otherwise stated) $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended				
Param	Device Characteristics	Min.	Тур†	Max.	Max.	Units		Conditions		
No.			- 71-1	+85°C	+125°C		VDD	Note		
	Power-down Base Current	(IPD) ⁽²⁾	•							
D026A*		—	250	—	—	μA	1.8	A/D Current (Note 1, Note 3),		
		-	250	—	—	μA	3.0	conversion in progress		
D026A*		_	280	—	—	μA	1.8	A/D Current (Note 1, Note 3),		
		_	280	—	—	μA	3.0	conversion in progress		
		—	280	_	—	μA	5.0			
D027		_	3.5	—	—	μA	1,8	Cap Sense Low Power		
		-	7	—	—	μA	3.0	Oscillator mode (Note 1)		
D027		_	22	—	—	μA	18	Cap Sense Low Power		
		_	26	—	—	цА	3.0	Oscillator mode (Note 1)		
		—	28	—	—	<μ A /	5.0			
D027A		-	4.2	—	- (-	-µA	1.8	Cap Sense Medium Power		
		_	6	—	-+(λή	× 3.0	Oscillator mode (Note 1)		
D027A		_	24	—	$\land - \land \land$	ha	1.8	Cap Sense Medium Power		
		—	29	<	(A)	μA	3.0	Oscillator mode (Note 1)		
		_	31	$\langle \rangle$	$\backslash \leftarrow$	μA	5.0			
D027B		_	12	\sim	\setminus \checkmark	μA	1.8	Cap Sense High Power		
		_	32	\mathcal{F}	~_	μA	3.0	Oscillator mode (Note 1)		
D027B		_	16	\searrow	—	μΑ	1.8	Cap Sense High Power		
		/	> 57	\searrow	—	μA	3.0	Oscillator mode (Note 1)		
		$-\langle \langle$	63	—		μA	5.0			
D028			6.9		—	μA	1.8	Comparator Current, Low Power		
		\bigwedge	7.0	—	—	μA	3.0	mode, one comparator enabled (Note 1)		
D028	\wedge	\geq	26			μA	1.8	Comparator Current, Low Power		
		<u> </u>	30		_	μA	3.0	mode, one comparator enabled		
		\rightarrow	32	_	_	μA	5.0	(Note 1)		
D028A	$ \land \lor $	_	6.6		_	μA	1.8	Comparator Current, Low Power mode, two comparators enabled (Note 1)		
		—	6.8	-	_	μA	3.0			
D028A		—	27	—	—	μA	1.8	Comparator Current, Low Power		
	\sim	_	31	_	—	μA	3.0	mode, two comparators enabled		
<	$(\langle \rangle)$	_	33	_	_	μA	5.0	(Note 1)		

These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: A/D oscillator source is FRC.

30.3 DC Characteristics: PIC16F/LF1825/1829-I/E (Power-Down) (Continued)

PIC16LF1	825/1829			rd Operation of the second sec	-	$-40^{\circ}C \le$	$TA \le +85^{\circ}$	erwise stated) C for industrial °C for extended	
PIC16F1825/1829				Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param	Device Characteristics	Tunt	Max.	Max.	Units		Conditions		
No.	Device Characteristics	Min.	Тур†	+85°C	+125°C	Units	Vdd	Note	
	Power-down Base Current	(IPD) ⁽²⁾							
D028B		_	24	_	_	μA	1.8	Comparator Current, High Power	
		—	25	—	—	μA	3.0	mode, one comparator enabled	
D028B		_	39		—	μA	1.8	Comparator Current, High Power	
			48	_	—	μA	3.0	mode, one comparator enabled	
		_	45	_	—	μA	5.0	(Note 1)	
D028C		—	40	_	—	μA	1.8	Comparator Current, High Power	
		_	41	_	_	μA	3.0	mode, two comparators enabled	
D028C		_	47		_	μA	1.8	Comparator Current, High Power	
		_	51		_	μA	3.0	mode, two comparators enabled	
		_	53		_	pa <	5.0	(Note 1)	

These parameters are characterized but not tested.

+ Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral ∆ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does for depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in tigh-inspectance state and tied to VDD.

3: A/D oscillator source is FRC.

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30.4 DC Characteristics: PIC16F/LF1825/1829-I/E

	DC CI	HARACTERISTICS		mperature	$-40^{\circ}C \le TA$	≤ +85°C	otherwise stated) C for industrial C for extended
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
	VIL	Input Low Voltage					
		I/O PORT:					
D030		with TTL buffer	—	_	0.8	V	$4.5V \le VDD \le 5.5V$
D030A					0.15 VDD	V	$1.8V \le VDD \le 4.5V$
D031		with Schmitt Trigger buffer			0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
		with I ² C™ levels	_	_	0.3 VDD	V	
		with SMBus levels		_	0.8	V	$2.7V \leq \sqrt{DQ} \leq 5.5V$
D032		MCLR, OSC1 (RC mode) ⁽¹⁾	_	_	0.2 VDD	V	
D033		OSC1 (HS mode)	_	_	0.3 VDD	V	\land
	VIH	Input High Voltage				^	
		I/O ports:		_	—		
D040		with TTL buffer	2.0	_	—	~~~	4,5 K ≤ VDD ≤ 5.5 V
D040A			0.25 VDD+	_	— _	N	$1.8V \leq VDD \leq 4.5V$
			0.8		\square		
D041		with Schmitt Trigger buffer	0.8 VDD	-	$\langle \langle \rangle$		$2.0V \leq V\text{DD} \leq 5.5V$
		with I ² C™ levels	0.7 VDD	—	$-/\langle$	V	
		with SMBus levels	2.1	- (($ (\mathcal{H}) $	V	$2.7V \leq V\text{DD} \leq 5.5V$
D042		MCLR	0.8 VDD		(\mathcal{F})	V	
D043A		OSC1 (HS mode)	0.7 VDD	TAN	\sim	V	
D043B		OSC1 (RC mode)	0.9 VDD	\searrow	—	V	(Note 1)
	lı∟	Input Leakage Current ⁽²⁾		//			
D060		I/O ports		$\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$	± 125 ± 1000	nA nA	Vss ≤ VPIN ≤ VDD, Pin at high- impedance at 85°C 125°C
D061		MCLR ⁽³⁾		√ ± 50	± 200	nA	Vss \leq VPIN \leq VDD at 85°C
5001	IPUR	Weak Pull-up Current	\sim	1 00	1200		
D070*			/25	100	200		VDD = 3.3V, VPIN = VSS
5010			25	140	300	μA	VDD = 5.0V, VPIN = VSS
	VOL	Output Low Voltage	\checkmark				
D080		I/O ports	_	_	0.6	V	IOL = 8mA, VDD = 5V IOL = 6mA, VDD = 3.3V IOL = 1.8mA, VDD = 1.8V
	Voh	Output High Voltage ⁽⁴⁾				1	
D090		I/O ports	Vdd - 0.7	_	_	v	IOH = 3.5mA, VDD = 5V IOH = 3mA, VDD = 3.3V IOH = 1mA, VDD = 1.8V
		Capacitive Loading Specs on	Output Pins				
D101*	CØSCZ	OSC2-pin	_	_	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D10(A*	610	All I/O pins	_	_	50	pF	
1*1		arameters are characterized but	not tested		1	ı .	1

√ These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined <u>as current sourced by the pin.</u>

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

DC CHA	ARACTE	RISTICS	Standard O Operating te				ess otherwise stated) 125°C
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
		Program Memory Programming Specifications					Ì
D110	VIHH	Voltage on MCLR/VPP/RA5 pin	8.0	_	9.0	V	(Note 3, Note 4)
D111	IDDP	Supply Current during Programming	—	—	10	mA	
D112		VDD for Bulk Erase	2.7	-	VDD max.	V	$\swarrow \!$
D113	VPEW	VDD for Write or Row Erase	VDD min.		VDD max.	√ ∕	
D114	IPPPGM	Current on MCLR/VPP during Erase/ Write	—		1.0 <	mA	
D115	IDDPGM	Current on VDD during Erase/Write	_		5.0	mA	
		Data EEPROM Memory		/	\bigcirc	\mathbf{i}	
D116	ED	Byte Endurance	100K	_ <		⁷ E/W	-40°C to +85°C
D117	Vdrw	VDD for Read/Write	VDD min.	$(\overline{\ }$	VDD max.	V	
D118	TDEW	Erase/Write Cycle Time	- //	4.0	5.0	ms	
D119	TRETD	Characteristic Retention	40	$\widehat{\langle}^{-}$	_	Year	Provided no other specifications are violated
D120	TREF	Number of Total Erase/Write Cycles before Refresh ⁽²⁾		∕10М	_	E/W	-40°C to +85°C
		Program Flash Memory	$\langle \rangle \rangle$				
D121	Eр	Cell Endurance	10K	—		E/W	-40°C to +85°C (Note 1)
D122	Vpr	VDD for Read	VDD min.	_	VDD max.	V	
D123	Tiw	Self-timed Write Cycle Time	_	2	2.5	ms	
D124	TRETD	Characteristic Retention	40			Year	Provided no other specifications are violated

30.5 Memory Programming Requirements

† Data in "Typ" column ts at 3,0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Self-write and Block Erase.

- 2: Refer to Section 11.2 "Using the Data EEPROM" for a more detailed discussion on data EEPROM endurance.
- 3: Required only it single-supply programming is disabled.

4: The MPLAB ICD 2 does not support variable VPP output. Circuitry to limit the MPLAB ICD 2 VPP voltage must be placed between the MPLAB ICD 2 and target system when programming or debugging with the MPLAB ICD 2.

30.6 Thermal Considerations

Param No.	Sym.	Characteristic	Тур.	Units	Conditions
TH01	θJA	Thermal Resistance Junction to Ambient	TBD	°C/W	8-pin PDIP package
			TBD	°C/W	8-pin SOIC package
		Ē	TBD	°C/W	8-pin DFN 3X3mm package
		Ē	TBD	°C/W	14-pin PDIP package
		Ī	TBD	°C/W	14-pin SOIC package (
		Ī	TBD	°C/W	14-pin TSSOP 4x4pm package
			TBD	°C/W	16-pin QFN 4X4mm package
TH02	θJC	Thermal Resistance Junction to Case	TBD	°C/W	8-pin PDIP package
			TBD	°C/W	8-pin SOIC package
			TBD	°C/W	8-pin DFN 3X3mm package
		Γ	TBD	°C/W	14-pin PDIP package
		Γ	TBD	°C/W	14 pin SQIC package
		Γ	TBD	°C/W <	14-pin TSSOP 4x4mm package
		Γ	TBD	°C/W	16-pin QFN 4X4mm package
TH03	TJMAX	Maximum Junction Temperature	150	19	\square
ГН04	PD	Power Dissipation	_	Ŵ	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation	- (W	PINTERNAL = IDD x VDD ⁽¹⁾
TH06	Pı/o	I/O Power Dissipation	— ((Ŵ	$PI/O = \Sigma (IOL * VOL) + \Sigma (IOH * (VDD - VOH)$
TH07	PDER	Derated Power	A	Ŵ	Pder = PDmax (ΤJ - ΤΑ)/θJA ⁽²⁾

Legend: TBD = To Be Determined

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

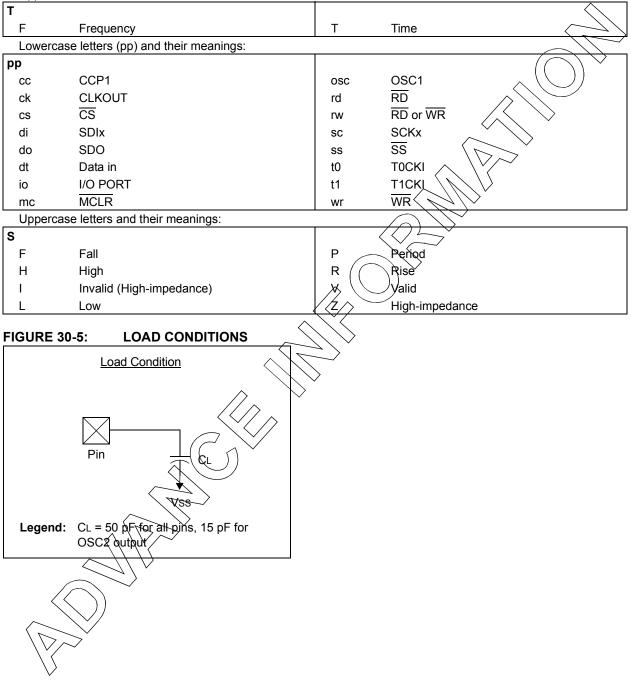
TA = Ambient Temperature
 TJ = Junction Temperature

DS41440A-page 366

30.7 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS



30.8 AC Characteristics: PIC16F/LF1825/1829-I/E

Q1 Q3 04 Q1 Q4 Q2 OSC1/CLKIN OS02 OS04 OS04 OS03 OSC2/CLKOUT (LP,XT,HS Modes) OSC2/CLKOUT (CLKOUT Mode) **CLOCK OSCILLATOR TIMING REQUIREMENTS** TABLE 30-1: Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^\circ C \le TA \le +125^\circ C$ Param Sym. Characteristic Min. Typ† Max Units Conditions No. External CLKIN Frequency⁽¹⁾ OS01 DC 0.5 MHz EC Oscillator mode (low) Fosc DC MHz EC Oscillator mode (medium) 4 DC 32 MHz EC Oscillator mode (high) Oscillator Frequency⁽¹⁾ LP Oscillator mode kHz 32.768 XT Oscillator mode 4 MHz 0.1 4 MHz HS Oscillator mode, VDD $\leq 2.7V$ 20 MHz HS Oscillator mode, VDD > 2.7V 1 DC 4 MHz RC Oscillator mode OS02 Tosc External CLKIN Period⁽¹ `₽7 LP Oscillator mode °0 μS 250 XT Oscillator mode s ns HS Oscillator mode 50 ____ ø ns 31.25 EC Oscillator mode x ns Oscillator Period M LP Oscillator mode 30.5 μs 250 10,000 XT Oscillator mode ns HS Oscillator mode 1,000 50 ns RC Oscillator mode 250 ns Instruction Cycle Time(1) OS03 TCY = Fosc/4 TCY 125 DC ns External CKKIN High, OS04' TosH.< 2 μs LP oscillator Tosl External CLKIN Low XT oscillator 100 ns 20 HS oscillator ns

FIGURE 30-6: CLOCK TIMING

These parameters are characterized but not tested.

External CLKIN Rise.

External CLKIN Fall

↑ ✓Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

s

s

x

ns

ns

ns

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

0

0

0

OS05'

TòsR,

τοsĥ

LP oscillator

XT oscillator

HS oscillator

TABLE 30-2: **OSCILLATOR PARAMETERS**

	d Operati ng Tempera	ng Conditions (unless otherwise stature $-40^{\circ}C \le TA \le +125^{\circ}C$	tated)					
Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Тур†	Max.	Units	Conditions
OS08	HFosc	Internal Calibrated HFINTOSC	±2%	_	16.0		MHz	$0^{\circ}C \le TA \le +60^{\circ}C, VDD \ge 2.5V$
		Frequency ⁽²⁾	±3%	_	16.0	—	MHz	$60^{\circ}C \le TA \le +85^{\circ}C, VDD \ge 2.5V$
			±5%	_	16.0	_	MHz	-40°C ≤ TA ≤ +125℃
OS08A	MFosc	Internal Calibrated MFINTOSC	±2%	_	500	_	kHz	$0^{\circ}C \le TA \le +60^{\circ}C$, $VDD \ge 2.5V$
		Frequency ⁽²⁾	±3%	-	500	—	kHz	60°C ≤ TA ≤ +85°C, VpD ≥ 2.5V
			±5%	_	500	—	kHz	-40°6 ≤ TA ≤ +125°C
OS09	LFosc	Internal LFINTOSC Frequency	—	_	31	—	kHz	-40°€ ≤ TA ≤ +)25°C
OS10*	TIOSC ST	HFINTOSC Wake-up from Sleep Start-up Time MFINTOSC	_	_	5	8	μs	
		Wake-up from Sleep Start-up Time	—	_	20	30	Jus	\bigvee

These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are t not tested.

- Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices. 2: To ensure these oscillator frequency tolerances, VDD and VSC must be capacitively decoupled as close to the device as
 - possible. 0.1 μ F and 0.01 μ F values in parallel are recommended.
 - 3: By design.

PLL CLOCK TIMING SPECIFICATIONS (VDD = 2.7V TO 5.5V) TABLE 30-3:

Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
F10	Fosc	Oscillator Frequency Range	4		8	MHz	
F11	Fsys	On-Chip VCO System Frequency	16	_	32	MHz	
F12	TRC	PLL Start-up Time (Lock Time)	—	—	2	ms	
F13*	ΔCLK	CLKOUT Stability (Jitter)	-0.25%	_	+0.25%	%	

These parameters are characterized but not tested.

Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance + only and are not tested.



PIC16F/LF1825/1829



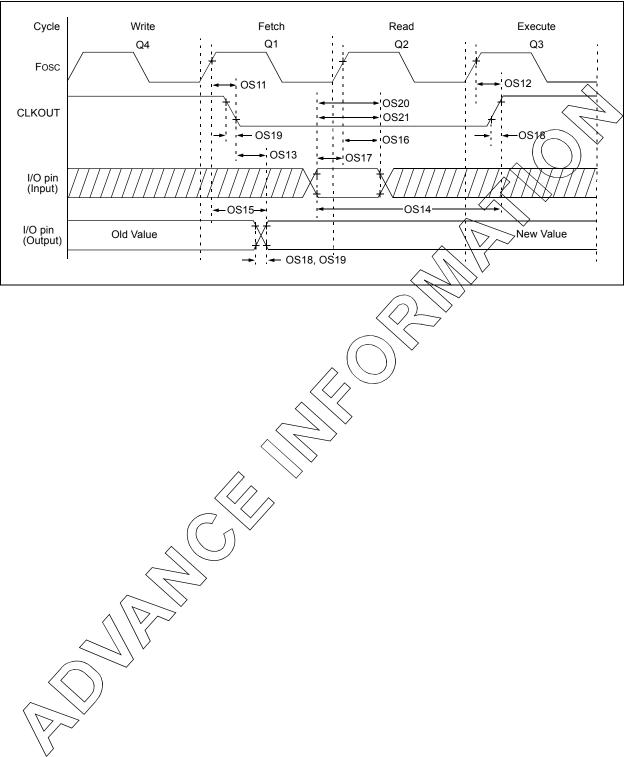


TABLE 30-4: CLKOUT AND I/O TIMING PARAMETERS
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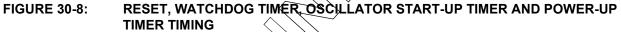
		g Conditions (unless otherwise stated) ure -40°C \leq TA \leq +125°C					
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
OS11	TosH2ckL	Fosc↑ to CLKOUT↓ ⁽¹⁾	—		70	ns	VDD = 3.3-5.0V
OS12	TosH2ckH	Fosc↑ to CLKOUT↑ ⁽¹⁾	—	_	72	ns	VDD = 3.3-5.0V
OS13	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	_	20	ns	$\langle n \rangle$
OS14	TioV2ckH	Port input valid before CLKOUT↑ ⁽¹⁾	Tosc + 200 ns	_	_	ns	\bigcirc
OS15	TosH2ioV	Fosc↑ (Q1 cycle) to Port out valid	—	50	70*	ns	VOD = 3.3-5.0V
OS16	TosH2iol	Fosc↑ (Q2 cycle) to Port input invalid (I/O in hold time)	50	_		ns	VDD = 3.3-5.0V
OS17	TioV2osH	Port input valid to Fosc↑ (Q2 cycle) (I/O in setup time)	20	-		en	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
OS18*	TioR	Port output rise time ⁽²⁾		90 55	140	~ris	VDD = 1.8V VDD = 3.3-5.0V
OS19*	TioF	Port output fall time ⁽²⁾		CO A	80	ns	VDD = 1.8V VDD = 3.3-5.0V
OS20*	Tinp	INT pin input high or low time	25) \rightarrow	_	ns	
OS21*	Tioc	Interrupt-on-change new input level time	25		_	ns	

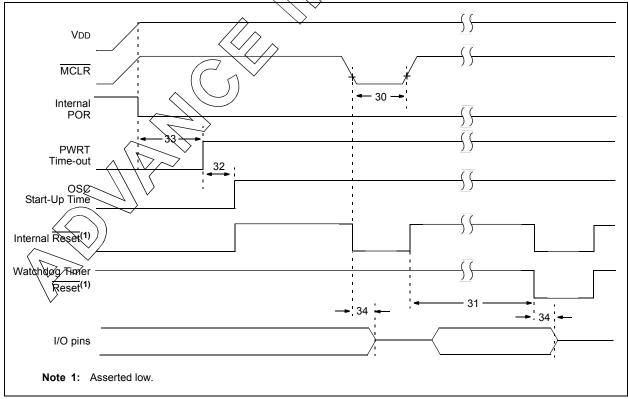
These parameters are characterized but not tested. †

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKØVT output is 4 x Tosc.

2: Includes OSC2 in CLKOUT mode.





PIC16F/LF1825/1829

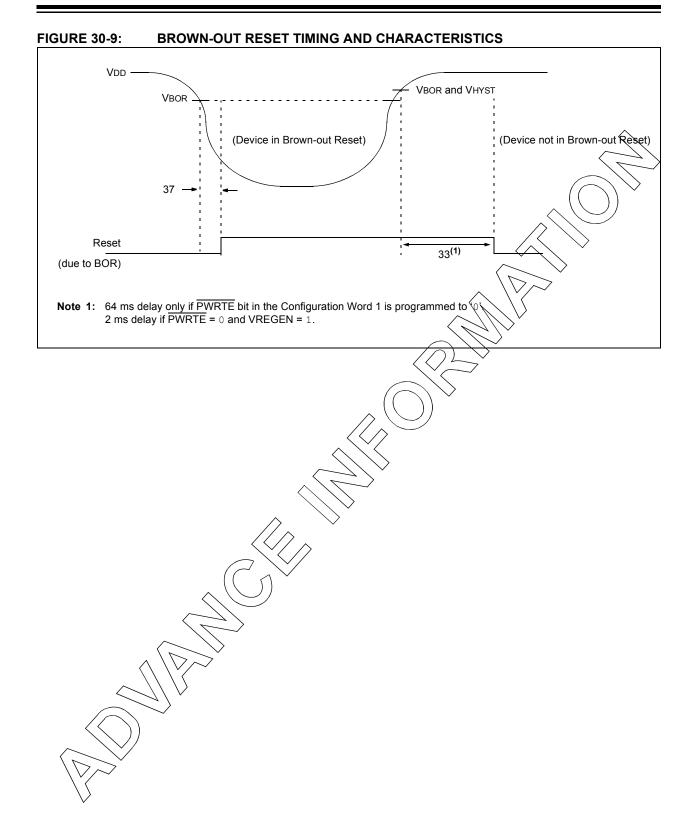


TABLE 30-5:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMERAND BROWN-OUT RESET PARAMETERS

Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2	_		μS	VDD = 3.3-5V, -40°C to +85°
			5	—	—	μS	VDD = 3.3-5V
31	TWDTLP	Low-Power Watchdog Timer	10	16	27	ms	VDD = 3.3V-5V,
		Time-out Period					1:16 Prescaler (u(sed)
32	Tost	Oscillator Start-up Timer Period ^{(1), (2)}	_	1024	—	Tosc	(Note 3)
33*	TPWRT	Power-up Timer Period, PWRTE = 0	40	65	140	ms	
34*	Tioz	I/O high-impedance from MCLR Low			2.0	μS	
		or Watchdog Timer Reset					\sim
35	VBOR	Brown-out Reset Voltage	2.38	2.5	2.65	ν.	BORV=2.5V
			1.80	1.9	2.05		BORV=1.9V
36*	VHYST	Brown-out Reset Hysteresis	0	25	50	Vm	40°C to +85°C
37*	TBORDC	Brown-out Reset DC Response	1	3	5	Jus	VDD ≤ VBOR
		Time			$\left \right $	$\rangle >$	

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- **Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
 - 2: By design.
 - **3:** Period of the slower clock.
 - **4:** To ensure these voltage tolerances, V_{DD} and Vss must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

FIGURE 30-10: TIMERO AND TIMER' EXTERNAL CLOCK TIMINGS

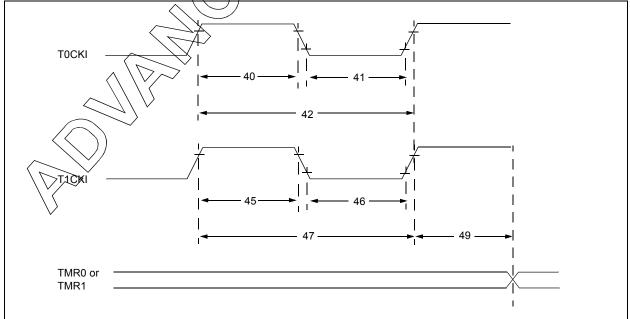


TABLE 30-6: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

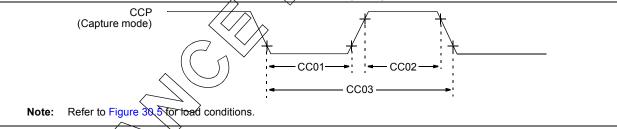
Standard Operating Conditions (unless otherwise stated)

	ng Temperatur	e -40°C ≤ TA :	≤+125°C						
Param No.	Sym.		Characteristic	C	Min.	Тур†	Max.	Units	Conditions
40*	T⊤0H	T0CKI High F	Pulse Width	No Prescaler	0.5 Tcy + 20	_	_	ns	
			With Prescaler		10	_		ns	\land
41*	TT0L	T0CKI Low P	ulse Width	No Prescaler	0.5 TCY + 20	_		ns	
				With Prescaler	10	—	_	ns	
42*	TT0P	T0CKI Period	1		Greater of:	—	_	ns	N = prescale value
			2		20 or <u>TCY + 40</u> N			\sim	(2, 4,, 256)
45*	TT1H	T1CKI High	Synchronous, No Prescaler		0.5 TCY + 20	_		/îs	
		Time	Synchronous, with Prescaler	3		—	- <	ns	\sim
			Asynchronous		30	_	44	ns	
46*	TT1L	T1CKI Low	Synchronous, N	lo Prescaler	0.5 TCY + 20	—	$\overline{\langle}$	/118	
		Time	Synchronous, v	vith Prescaler	15	$-\langle$	\mathcal{I}	ns	
			Asynchronous		30	Ą,	(H)	ns	
47*	TT1P	T1CKI Input Period	Synchronous		Greater of: 30 or <u>Tcy + 40</u>	T T		ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		60	$\langle - \rangle$		ns	
48	F⊤1		ator Input Frequ abled by setting	, ,	32.4	32.768	33.1	kHz	
49*	TCKEZTMR1	Delay from E Increment	xternal Clock Ec	lge to Timer	2 TOSC	—	7 Tosc	—	Timers in Sync mode

These parameters are characterized but not tested. <

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not † tested.

CAPTURE/COMPARE/PWM TIMINGS (CCP) FIGURE 30-11:



CAPTURE/COMPARE/PWM REQUIREMENTS (CCP) **TABLE 30-7:**

		perature $-40^{\circ}C \le TA \le +1$		i)				
Param No.	Sym.	Characteri	stic	Min.	Тур†	Max.	Units	Conditions
CC0(1*	Tecl	CCP Input Low Time	No Prescaler	0.5TCY + 20		—	ns	
	\bigtriangledown	}	With Prescaler	20		-	ns	
CC02*	Тссн	CCP Input High Time	No Prescaler	0.5TCY + 20		-	ns	
	\vee		With Prescaler	20	_	_	ns	
CC03*	TccP	CCP Input Period		<u>3Tcy + 40</u> N	—	-	ns	N = prescale value (1, 4 or 16)

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 30-8: PIC16F/LF1825/1829 A/D CONVERTER (ADC) CHARACTERISTICS:

	•	rating Conditions (unless otherwork operature $-40^{\circ}C \le TA \le +125^{\circ}C$	ise state	ed)			
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
AD01	NR	Resolution	—	_	10	bit	
AD02	EIL	Integral Error	_		±1.7	LSb	VREF = 3.0V
AD03	Edl	Differential Error	-	—	±1	LSb	No missing codes VREF = 3.0V
AD04	EOFF	Offset Error	—	—	±2	LSb	VREF = 3.0V
AD05	Egn	Gain Error	-	_	±1.5	LSb	VREF = 3.0V
AD06	VREF	Reference Voltage ⁽³⁾	1.8		Vdd	V	VREF = (VREF+ minus VREF-) (NOTE 5)
AD07	VAIN	Full-Scale Range	Vss		VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	-	_	10	kΩ	Can go higher if external 0.01μF capacitor is present on input pin.

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input vottage and has no missing codes.

3: ADC VREF is from external VREF, VDD pin or FVR, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage correct. The power-down current specification includes any such leakage from the ADC module.

5: FVR voltage selected must be 2.048V or 4.096V.

TABLE 30-9: PIC16F/LF1825/1829 A/D CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)

Operatin	Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$								
Param No.	Sym.	Characteristic	Min.	न्द्र	Max.	Units	Conditions		
AD130*	TAD	A/D Clock Period	1.0) -	9.0	μS	Tosc-based		
		A/D Internal RC Oscillator Period	1.0	[*] 1.6	6.0	μS	ADCS<1:0> = 11 (ADRC mode)		
AD131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	V	11	_	TAD	Set GO/DONE bit to conversion complete		
AD132*	TACQ	Acquisition Time	—	5.0	_	μS			

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The ADRES register may be read on the following TCY cycle.

PIC16F/LF1825/1829

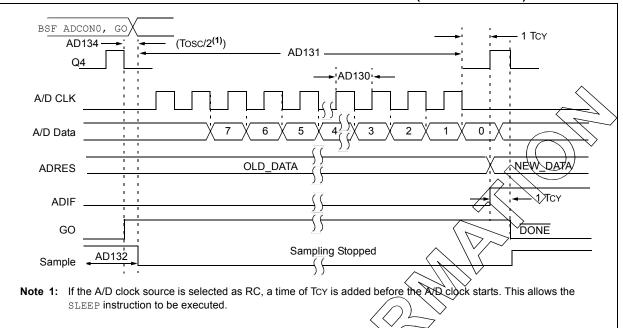
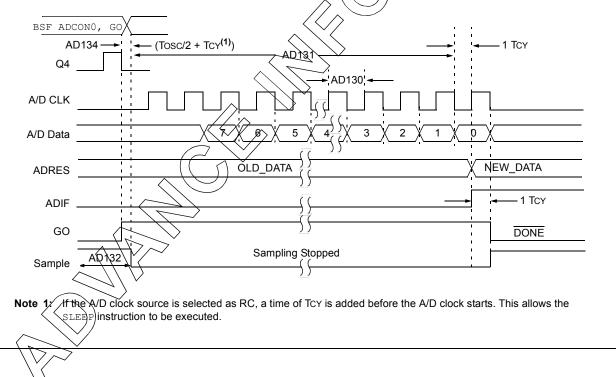


FIGURE 30-12: PIC16F/LF1825/1829 A/D CONVERSION TIMING (NORMAL MODE)





Operating	Conditions	: 1.8V < VDD < 5.5V, -40°C < TA <	+125°C (u	nless othe	erwise state	d).	
Param No.	Sym.	Characteristics	Min.	Тур.	Max.	Units	Comments
CM01	VIOFF	Input Offset Voltage		±7.5	±60	mV	
CM02	VICM	Input Common Mode Voltage	0	—	Vdd	V	
CM03	CMRR	Common Mode Rejection Ratio	_	50	_	dB	
CM04A		Response Time Rising Edge	—	400	800	ns	High Power Mode (NØTE 1)
CM04B		Response Time Falling Edge	_	200	400	ns	High Power Mode
CM04C	- Tresp	Response Time Rising Edge	_	1200	(ns	Low Power Mode (NOTE 1)
CM04D		Response Time Falling Edge	—	550		Tis/	Low Power Mode (NOTE 1)
CM04	TRESP	Response Time	_	150	×400	∕∕ns	NOTE 1
CM05	Тмс2о∨	Comparator Mode Change to Output Valid*	—		TO	μs	
CM06	CHYSTER	Comparator Hysteresis	—	<u> </u>	\sim	mV	NOTE 2

TABLE 30-10: COMPARATOR SPECIFICATIONS

These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at VDD/2, while the other input transitions from Vss to VDD.

2: Comparator Hysteresis is available when the CxAYS bit of the CMxCON0 register is enabled.

TABLE 30-11: DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating	Operating Conditions: 1.8V < VDD < 5.5V, -40°℃ < TA < +125°C (unless otherwise stated).								
Param No.	Sym.	Characteristics	Min.	Тур.	Max.	Units	Comments		
DAC01*	CLSB	Step Size ⁽²⁾	—	VDD/32		V			
DAC02*	CACC	Absolute Accuracy	_	—	± 1/2	LSb			
DAC03*	CR	Unit Resistor Value (R)	_	TBD	_	Ω			
DAC04*	CST	Settling Time(1)	—	—	10	μS			

* These parameters are characterized but not tested.

Legend: TBD = To Be Determined

Note 1: Settling time measured while DACR<4:0> transitions from '0000' to '1111'.

TABLE 30-12: PIC16F/LF1825/1829 LOW DROPOUT (LDO) REGULATOR CHARACTERISTICS:

	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$								
Param No.	S	ým.	>	Characteristic Min. Typ† Max. Units Conditions				Conditions	
LD001	$\mathbf{\hat{v}}$,	LDO R	Regulation Voltage	—	3.2	—	V	
LD002			LDO E	external Capacitor	0.1	-	1	μF	

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16F/LF1825/1829

FIGURE 30-14: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

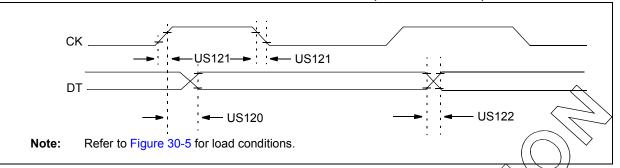


TABLE 30-13: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

	Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$									
Param. No.	Symbol	Characteristic		Min. <	Max.	Units	Conditions			
US120	TCKH2DTV	SYNC XMIT (Master and Slave)	3.0-5.5V	H 1/	7 80	ns				
		Clock high to data-out valid	1.8-5.5V		100	ns				
US121	TCKRF	Clock out rise time and fall time	3.0-5.5V <	\bigtriangledown	y 45	ns				
		(Master mode)	1.8-5.5∀	\searrow	50	ns				
US122	TDTRF	Data-out rise time and fall time	3.0-5.5V) —	45	ns				
			1.8-5.5	/ _	50	ns				

FIGURE 30-15: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

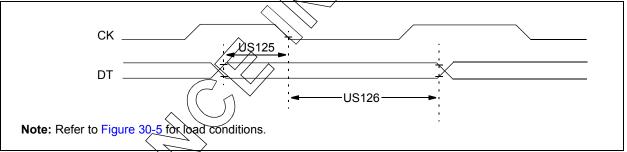
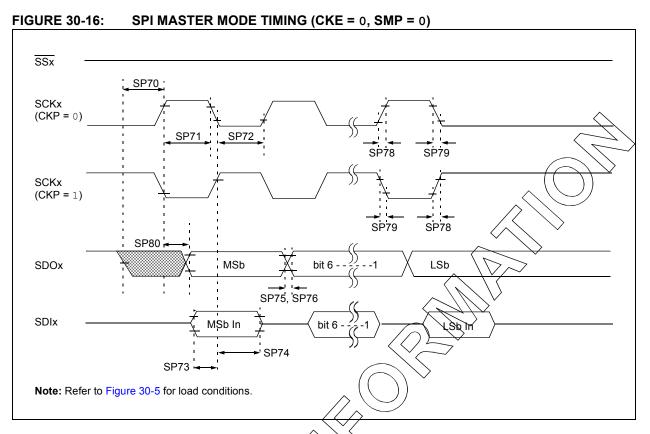
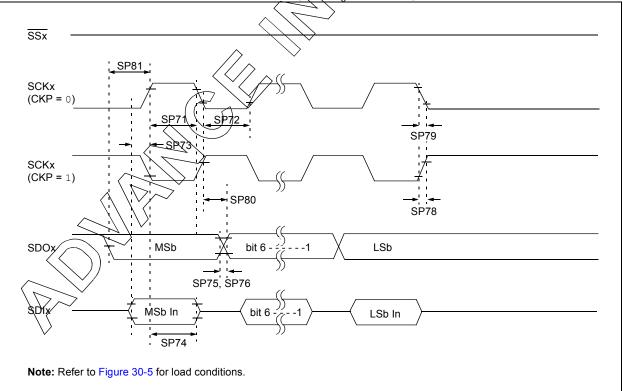


TABLE 30-14: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating Temperature \checkmark -40°C \leq TA \leq +125°C								
Param. No.	Characteristic	Min.	Max.	Units	Conditions			
US125 TDTV20	SYNC RCV (Master and Slave) Data-hold before CK ↓ (DT hold time)	10	_	ns				
	L Data-hold after CK \downarrow (DT hold time)	15	_	ns				







PIC16F/LF1825/1829

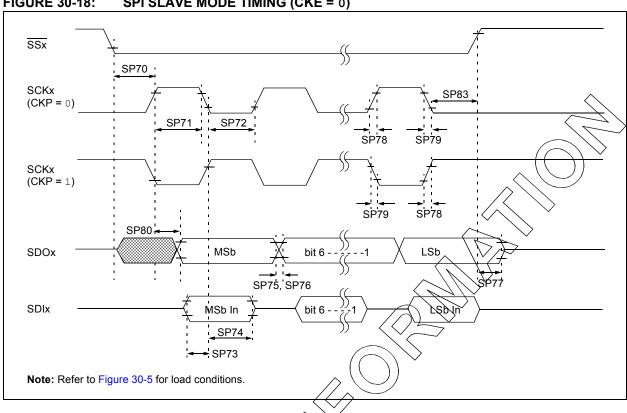
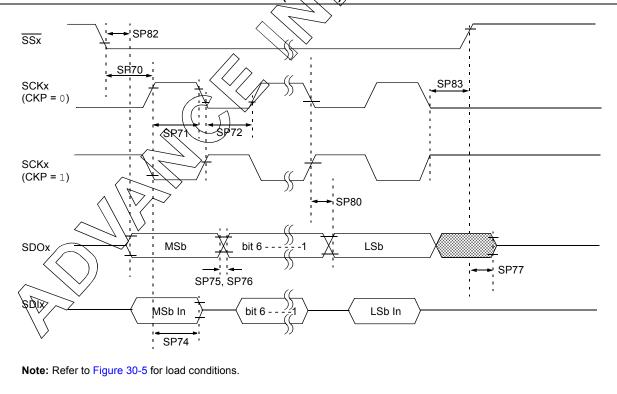


FIGURE 30-18: SPI SLAVE MODE TIMING (CKE = 0)



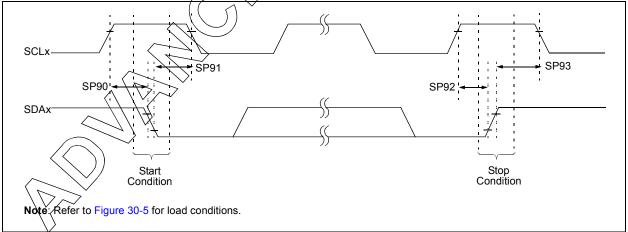


Param No.	Symbol	Characteristic	Min.	Тур†	Max.	Units	Conditions	
SP70*	TssL2scH, TssL2scL	SSx↓ to SCKx↓ or SCKx↑ input		Тсү	_	—	ns	
SP71*	TscH	SCKx input high time (Slave mo	de)	Tcy + 20	_	_	ns	\land
SP72*	TscL	SCKx input low time (Slave mod	e)	Tcy + 20		_	ns	$\langle \gamma \rangle$
SP73*	TDIV2scH, TDIV2scL	Setup time of SDIx data input to	SCKx edge	100		—	ns	\sum
SP74*	TscH2diL, TscL2diL	Hold time of SDIx data input to S	100		-	ns	\mathcal{D}	
SP75*	TDOR	SDO data output rise time	3.0-5.5V	—	10	/25	ns	
			1.8-5.5V	_	25	50	ns	
SP76*	TdoF	SDOx data output fall time		_	10 5	25	, ns	
SP77*	TssH2doZ	SSx↑ to SDOx output high-impe	dance	10 🧹	$\overline{\langle - \rangle}$	50	ns	
SP78*	TscR	SCKx output rise time	3.0-5.5V	-~	/ 10	25	ns	
		(Master mode)	1.8-5.5V	_	25	50	ns	
SP79*	TscF	SCKx output fall time (Master mo	ode)		$\overline{>}10$	25	ns	
SP80*	TscH2doV,	SDOx data output valid after	3.0-5.5V	$\langle \langle \langle \rangle \rangle$	_	50	ns	
	TscL2DoV	SCKx edge	1.8-5.5V	\bigtriangledown		145	ns	
SP81*	TDOV2scH, TDOV2scL	SDOx data output setup to SCK	k edge	Тсу		_	ns	
SP82*	TssL2doV	SDOx data output valid after SS	_		50	ns		
SP83*	TscH2ssH, TscL2ssH	SSx ↑ after SCKx edge	1.5Tcy + 40		—	ns		

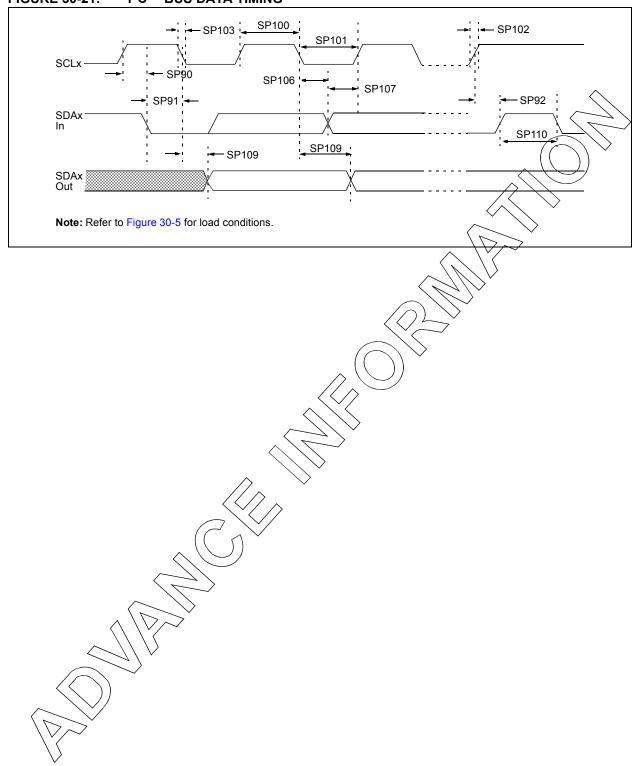
TABLE 30-15: SPI MODE REQUIREMENTS

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested. t

I²C™ BUS START/STOP BITS TIMING **FIGURE 30-20:**



PIC16F/LF1825/1829



Param. No.	Symbol	Characte	eristic	Min.	Max.	Units	Conditions
SP100*	0* Тнідн Clock high time 100 kHz r		100 kHz mode	4.0	_	μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6		μS	Device must operate at a minimum of 10 MHz
			SSPx module	1.5Tcy	_	_	
SP101*	101* TLOW		100 kHz mode	4.7		μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3		μS	Device must operate at a minimum of 10 MHz
			SSPx module	1.5Tcy	_	_	
SP102*	TR	SDAx and SCLx	100 kHz mode	_	1000	ns r	\searrow
		rise time	400 kHz mode	20 + 0.1Св	300	ns	CF is specified to be from 10-400 pF
SP103*	TF	SDAx and SCLx fall time	100 kHz mode	_	250	Ins	
			400 kHz mode	20 + 0.1Св	250	N S	CB is specified to be from 10-400 pF
SP106*	THD:DAT	Data input hold time	100 kHz mode	0	$\mathbf{\tilde{\mathbf{x}}}$	ns	
			400 kHz mode	Ø	0.9	μS	
SP107*	TSU:DAT	Data input setup	100 kHz mode	> 250) —	ns	(Note 2)
		time	400 kHz mode	100	_	ns	
SP109*	ΤΑΑ	Output valid from	100 kHz mode	Х́—	3500	ns	(Note 1)
		clock	400 kHz mode	\sim	_	ns	
SP110*	TBUF	Bus free time	100 kHz mode	4.7	_	μS	Time the bus must be free
			400 kHz mode	1.3	_	μS	before a new transmission can start
SP111	Св	Bus capacitive loading	$\dot{\lambda}$		400	pF	

TABLE 30-16: I²C[™] BUS DATA REQUIREMENTS

These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCLx to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) ²C[™] bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement (SU:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCLx signal. If such a device does stretch the low period of the SCLx signal, it must output the next data bit to the SDAx line TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCLx line is released.

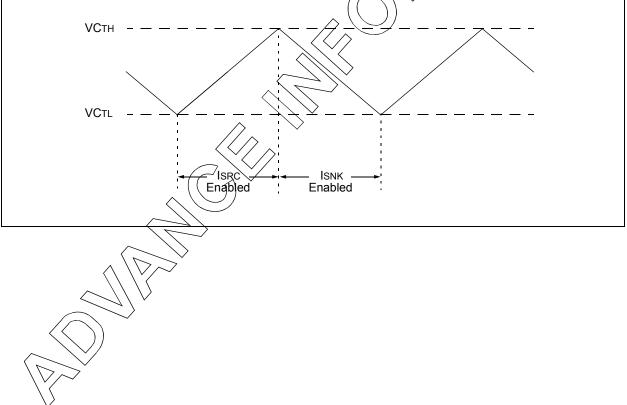
Param. No.	Symbol	Characteristic		Min.	Тур†	Max.	Units	Conditions
CS01	ISRC	Current Source	High	-3	-8	-15	μΑ	
			Medium	-0.8	-1.5	-3	μA	
			Low	-0.1	-0.3	-0.4	μA	
CS02	Isnk	Current Sink	High	2.5	7.5	14	μA	$\langle \rangle$
			Medium	0.6	1.5	2.9	μA	
			Low	0.1	0.25	0.6	μA	
CS03	VСтн	Cap Threshold		—	0.8	_	mV	
CS04	VCTL	Cap Threshold		—	0.4	_	mV	$\langle \rangle \rangle$
CS05	VCHYST	CAP HYSTERESIS	High	350	525	725	mV	$\langle \! \backslash \! \rangle $
		(VCTH-VCTL)	Medium	250	375	500	mV	\square
			Low	175	300	425	mV	\vee

TABLE 30-17: CAP SENSE OSCILLATOR SPECIFICATIONS

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.





31.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

Graphs and charts are not available at this time.

NOTES:

1.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers and dsPIC[®] digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB[®] IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C for Various Device Families
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICkit™ 3 Debug Express
- Device Programmers
 - PICkit[™] 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

1.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows[®] operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- · Mouse over variable inspection
- Drag and drop variables from source to watch windows
- · Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- · Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

1.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

1.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

1.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

1.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

1.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command line interface
- · Rich directive set
- Flexible macro language
- · MPLAB IDE compatibility

1.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC[®] DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

1.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with incircuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

1.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC[®] Flash microcontrollers and dsPIC[®] DSCs with the powerful, yet easyto-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

1.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC[®] and dsPIC[®] Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming[™].

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

1.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit[™] 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit[™] 2 enables in-circuit debugging on most PIC[®] microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

1.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

1.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

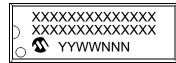
Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

33.0 PACKAGING INFORMATION

33.1 Package Marking Information

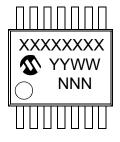
14-Lead PDIP



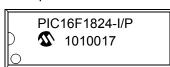
14-Lead SOIC (.150")



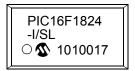
14-Lead TSSOP



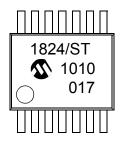
Example



Example



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	be carrie	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for customer-specific information.

* Standard PICmicro[®] device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

33.2 Package Marking Information

16-Lead QFN (4x4x0.9 mm)



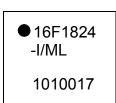
20-Lead PDIP



20-Lead SOIC (.300")



Example



Example



Example

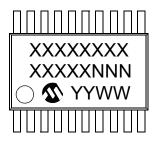


Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	be carried	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available for customer-specific information.

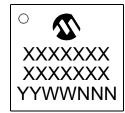
* Standard PICmicro[®] device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

33.3 Package Marking Information

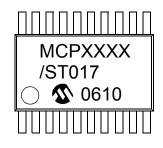
20-Lead TSSOP



20-Lead QFN (4x4)



Example



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	be carrie	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for customer-specific information.

* Standard PICmicro[®] device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

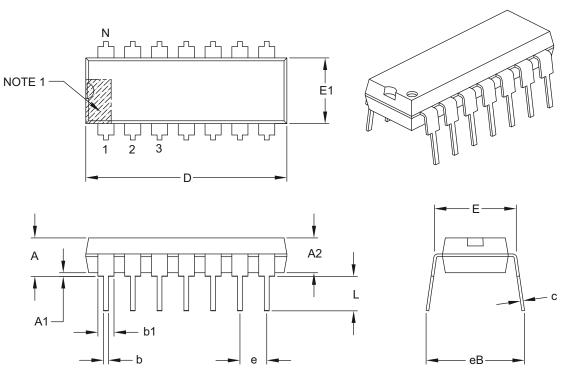
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33.4 Package Details

The following sections give the technical details of the packages.

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES		
Dimensio	n Limits	MIN	NOM	MAX	
Number of Pins	Ν	14			
Pitch	е	.100 BSC			
Top to Seating Plane	Α	-	-	.210	
Molded Package Thickness	A2	.115	.130	.195	
Base to Seating Plane	A1	.015	-	_	
Shoulder to Shoulder Width	Е	.290	.310	.325	
Molded Package Width	E1	.240	.250	.280	
Overall Length	D	.735	.750	.775	
Tip to Seating Plane	L	.115	.130	.150	
Lead Thickness	С	.008	.010	.015	
Upper Lead Width	b1	.045	.060	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eB	-	_	.430	

Notes:

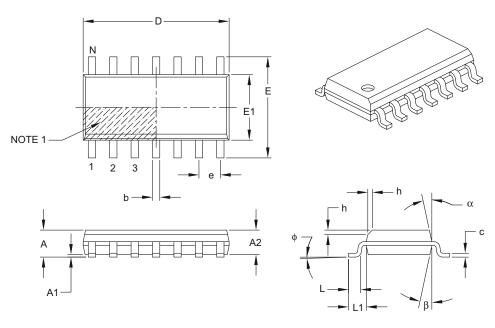
- 1. Pin 1 visual index feature may vary, but must be located with the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
D	imension Limits	MIN	NOM	MAX
Number of Pins	N	14		
Pitch	е	1.27 BSC		
Overall Height	А	_	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	ф	0°	-	8°
Lead Thickness	С	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	_	15°
Mold Draft Angle Bottom	β	5°	_	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

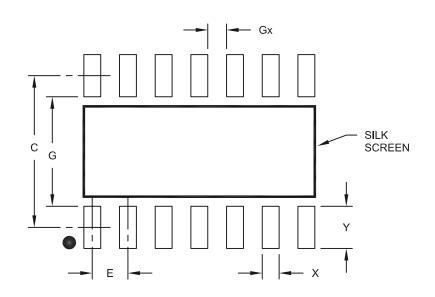
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units MILLIMETERS		S	
Dimensior	Dimension Limits		NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	С		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

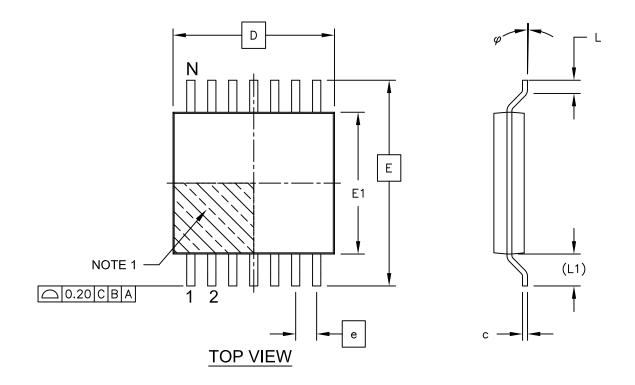
1. Dimensioning and tolerancing per ASME Y14.5M

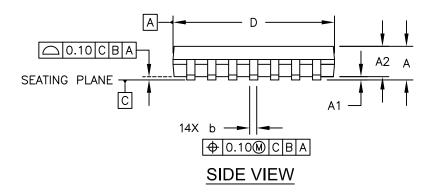
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

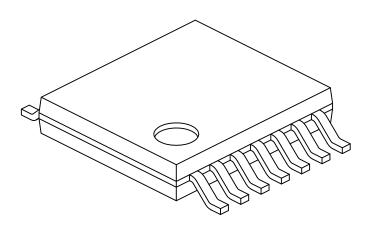




Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	е	0.65 BSC		
Overall Height	Α	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)	1.00 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or

protrusions shall not exceed 0.15mm per side.

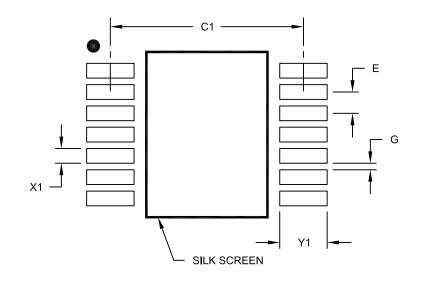
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units		/ILLIMETER	S
Dimension	Dimension Limits		NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

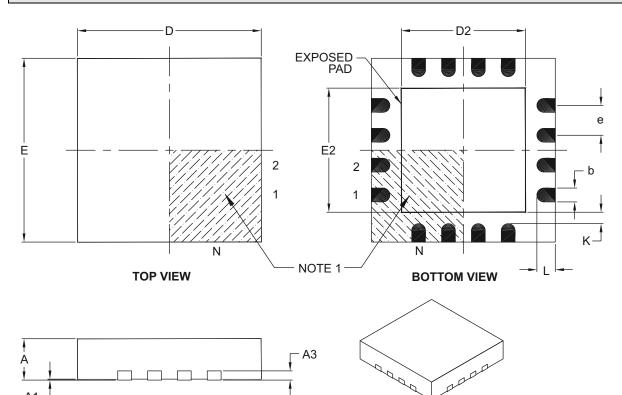
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	
Number of Pins	N		16		
Pitch	е		0.65 BSC		
Overall Height	А	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3		0.20 REF		
Overall Width	E		4.00 BSC		
Exposed Pad Width	E2	2.50	2.65	2.80	
Overall Length	D		4.00 BSC		
Exposed Pad Length	D2	2.50	2.65	2.80	
Contact Width	b	0.25	0.30	0.35	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	K	0.20	_	-	

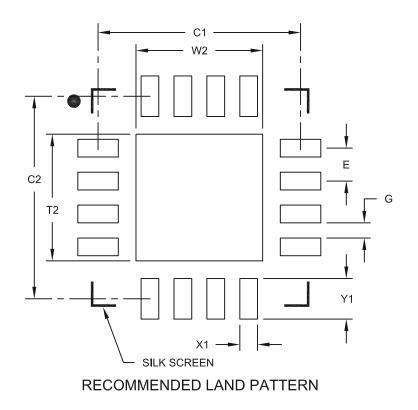
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

16-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		Ν	ILLIMETER	S
Dimension	ı Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X28)	X1			0.35
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.30		

Notes:

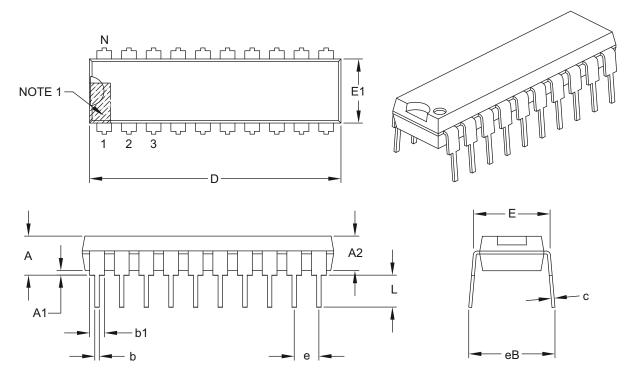
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2127A

20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimen	ision Limits	MIN	NOM	MAX
Number of Pins	Ν		20	
Pitch	е		.100 BSC	
Top to Seating Plane	А	_	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

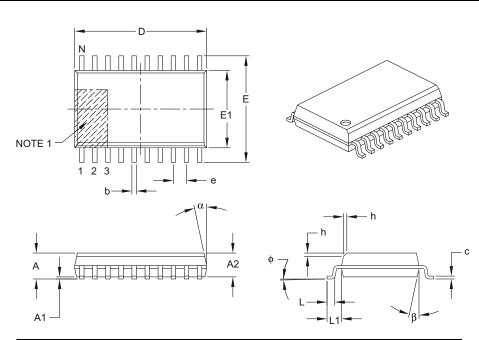
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

20-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	5
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		1.27 BSC	
Overall Height	А	—	—	2.65
Molded Package Thickness	A2	2.05	—	—
Standoff §	A1	0.10	—	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1		7.50 BSC	
Overall Length	D		12.80 BSC	
Chamfer (optional)	h	0.25	—	0.75
Foot Length	L	0.40	—	1.27
Footprint	L1		1.40 REF	
Foot Angle	φ	0°	—	8°
Lead Thickness	С	0.20	—	0.33
Lead Width	b	0.31	_	0.51
Mold Draft Angle Top	α	5°	_	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

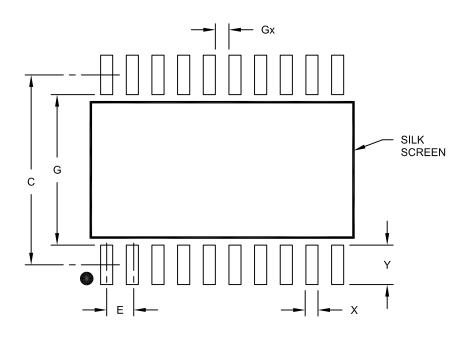
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-094B

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units		ILLIMETER	S
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		9.40	
Contact Pad Width (X20)	X			0.60
Contact Pad Length (X20)	Y			1.95
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.45		

Notes:

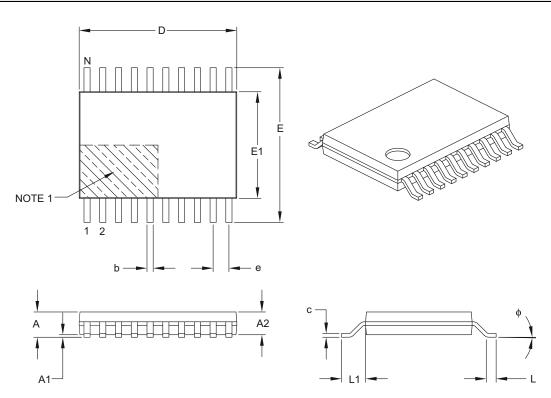
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2094A

20-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
Dimensio	on Limits	MIN	NOM	MAX	
Number of Pins	Ν		20		
Pitch	е		0.65 BSC		
Overall Height	Α	_	-	1.20	
Molded Package Thickness	A2	0.80	1.00	1.05	
Standoff	A1	0.05	-	0.15	
Overall Width	E		6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50	
Molded Package Length	D	6.40	6.50	6.60	
Foot Length	L	0.45	0.60	0.75	
Footprint	L1		1.00 REF		
Foot Angle	¢	0°	-	8°	
Lead Thickness	С	0.09	-	0.20	
Lead Width	b	0.19	-	0.30	

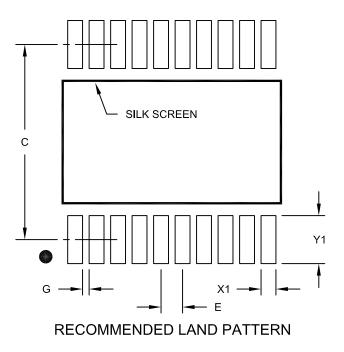
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
 Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-088B

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		/ILLIMETER	S
Dimension	Dimension Limits		NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		5.90	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

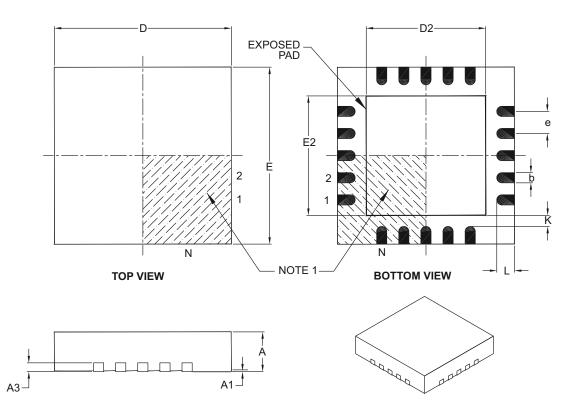
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2088A

20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	;
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	К	0.20	-	_

Notes:

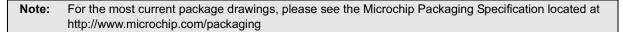
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

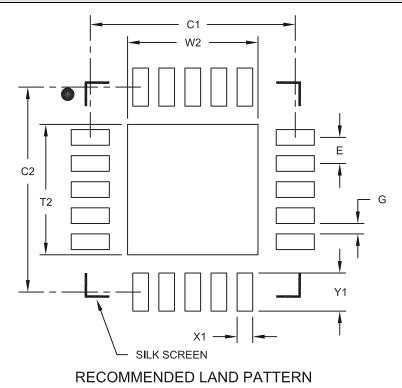
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

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20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN] With 0.40 mm Contact Length





	11.14			0
	Units	N	/ILLIMETER	S
Dimensior	l Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		3.93	
Contact Pad Spacing	C2		3.93	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.73
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

Original release (08/2010).

APPENDIX B: MIGRATING FROM OTHER PIC[®] DEVICES

This shows a comparison of features in the migration from the PIC16F648 device to the PIC16F/LF1825/1829 family of devices.

This section provides comparisons when migrating from other similar $\text{PIC}^{\textcircled{0}}$ devices to the <code>PIC16F/LF1825/1829</code> family of devices.

B.1 PIC16F648A to PIC16F1825/1829

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F648A	PIC16F1825/1829
Max. Operating Speed	20 MHz	32 MHz
Max. Program Memory (Words)	4K	8K
Max. SRAM (Bytes)	256	1024
Max. EEPROM (Bytes)	256	256
A/D Resolution	10-bit	10-bit
Timers (8/16-bit)	2/1	4/1
Brown-out Reset	Y	Y
Internal Pull-ups	RB<7:0>	PIC16F1825: RA<5:0>, RC<5:0> PIC16F1829: RA<5:0>, RB<7:4>, RC<7:0>
Interrupt-on-change	RB<7:4>	PIC16F1825: RA<5:0>, Edge Selectable PIC16F1829: RA<5:0>, RB<7:4>, Edge Selectable
Comparator	2	2
AUSART/EUSART	1/0	0/1
Extended WDT	N	Y
Software Control Option of WDT/BOR	N	Y
INTOSC Frequencies	48 kHz or 4 MHz	31 kHz - 32 MHz
Clock Switching	Y	Y
Capacitive Sensing	N	Y
CCP/ECCP	2/0	2/2
Enhanced PIC16 CPU	Ν	Y
MSSPx/SSPx	0	2/0
Reference Clock	N	Y
Data Signal Modulator	Ν	Y
SR Latch	N	Y
Voltage Reference	Ν	Y
DAC	Y	Y

NOTES:

INDEX

F	۱.
-	•

A/D	
Specifications	. 375
Absolute Maximum Ratings	353
AC Characteristics	
Industrial and Extended	. 368
Load Conditions	. 367
ACKSTAT	
ACKSTAT Status Flag	. 280
ADC	
Acquisition Requirements	
Associated registers	. 164
Block Diagram	
Calculating Acquisition Time	
Channel Selection	
Configuration	
Configuring Interrupt	
Conversion Clock	
Conversion Procedure	
Internal Sampling Switch (Rss) Impedance	
Interrupts	
Operation	
Operation During Sleep	
Port Configuration	
Reference Voltage (VREF)	
Source Impedance	
Special Event Trigger	
Starting an A/D Conversion	
ADCON0 Register	
ADCON1 Register	
ADDFSR	
ADDWFC	
ADRESH Register	
ADRESH Register (ADFM = 0)	
ADRESH Register (ADFM = 1)	
ADRESL Register (ADFM = 0)	
ADRESL Register (ADFM = 1)	
Alternate Pin Function	. 124
Analog-to-Digital Converter. See ADC ANSELA Register	120
ANSELA Register	
ANSELD Register	
APFCON0 Register	
APFCONU Register	
ASSembler	. 120
MPASM Assembler	388
В	

BAUDCON Register	
BF	
BF Status Flag	
Block Diagram	
Capacitive Sensing	327, 328
Block Diagrams	
(CCP) Capture Mode Operation	
ADC	151
ADC Transfer Function	
Analog Input Model	163, 183
CCP PWM	
Clock Source	
Comparator	
Compare	
Crystal Operation	60, 61

166
300
61
69
123
87
88
22
14
226
60
187
191
6, 197, 198
203
147
166
81
344
319
81
373
372

С

C Compilers	
MPLAB C18	
CALL	
CALLW	
Capacitive Sensing	
Associated registers w/ Capacitive Sensing	
Specifications	384
Capture Module. See Enhanced Capture/Compare/ PWM(ECCP)	
Capture/Compare/PWM	. 217
Capture/Compare/PWM (CCP)	
Associated Registers w/ Capture	. 219
Associated Registers w/ Compare	. 221
Associated Registers w/ PWM 225	, 239
Capture Mode	. 218
CCPx Pin Configuration	. 218
Compare Mode	220
CCPx Pin Configuration	220
Software Interrupt Mode 218	, 220
Special Event Trigger	220
Timer1 Mode Resource 218	
Prescaler	218
PWM Mode	
Duty Cycle	223
Effects of Reset	. 225
Example PWM Frequencies and	
Resolutions, 20 MHZ	. 224
Example PWM Frequencies and	
Resolutions, 32 MHZ	. 224
Example PWM Frequencies and	
Resolutions, 8 MHz	224
Operation in Sleep Mode	225
Resolution	. 224
System Clock Frequency Changes	. 225
PWM Operation	
PWM Overview	
PWM Period	

PIC16F/LF1825/1829

DW/M Cature 000
PWM Setup
CCP1CON Register
CCPR1H Register
CCPR1L Register
CCPTMRS Register
CCPxAS Register
CCPxCON (ECCPx) Register
CLKRCON Register
Clock Accuracy with Asynchronous Operation
Clock Sources
External Modes59
EC
HS
LP
OST60
RC61
XT
Internal Modes62
HFINTOSC62
Internal Oscillator Clock Switch Timing64
LFINTOSC63
MFINTOSC62
Clock Switching
CMOUT Register
CMxCON0 Register
CMxCON1 Register
Code Examples
A/D Conversion
Changing Between Capture Prescalers
Initializing PORTA
Initializing PORTB
Initializing PORTC138
Write Verify 119
Writing to Flash Program Memory117
Comparator
Associated Registers
Operation177
Comparator Module 177
Cx Output State Versus Input Conditions
Comparator Specifications
Comparators
C2OUT as T1 Gate
Compare Module. See Enhanced Capture/
Compare/PWM (ECCP)
CONFIG1 Register
5
CONFIG2 Register
CPSCON0 Register
CPSCON1 Register
Customer Change Notification Service
Customer Notification Service
Customer Support

D

DACCON0 (Digital-to-Analog Converter Control 0)	
Register	168
DACCON1 (Digital-to-Analog Converter Control 1)	
Register	168
Data EEPROM Memory	109
Associated Registers	122
Code Protection	110
Reading	110
Writing	
Data Memory	25
DC and AC Characteristics	385
DC Characteristics	
Extended and Industrial	364

Industrial and Extended	356
Development Support	
Device Configuration	
Code Protection	55
Configuration Word	
User ID	55, 56
Device Overview	13, 105
Digital-to-Analog Converter (DAC)	165
Associated Registers	169
Effects of a Reset	166
Specifications	

Е

ECCP/CCP. See Enhanced Capture/Compare/PWM	
EEADR Registers	109
EEADRH Registers	109
EEADRL Register	120
EEADRL Registers	
EECON1 Register	
EECON2 Register	
EEDATH Register	
EEDATL Register	
EEPROM Data Memory	120
	440
Avoiding Spurious Write	
Write Verify	119
Effects of Reset	
PWM mode	
Electrical Specifications	
Enhanced Capture/Compare/PWM (ECCP)	
Enhanced PWM Mode	226
Auto-Restart	235
Auto-shutdown	234
Direction Change in Full-Bridge Output Mode.	232
Full-Bridge Application	
Full-Bridge Mode	
Half-Bridge Application	
Half-Bridge Application Examples	
Half-Bridge Mode	
	229
Output Relationships (Active-High and	007
Active-Low)	
Output Relationships Diagram	
Programmable Dead Band Delay	
Shoot-through Current	
Start-up Considerations	
Specifications	374
Enhanced Mid-range CPU	21
Enhanced Universal Synchronous Asynchronous	
Receiver Transmitter (EUSART)	299
Errata	
EUSART	299
Associated Registers	
Baud Rate Generator	312
Asynchronous Mode	
12-bit Break Transmit and Receive	
	519
Associated Registers	~~ -
Receive	
Transmit	
Auto-Wake-up on Break	
Baud Rate Generator (BRG)	
Clock Accuracy	308
Receiver	
Setting up 9-bit Mode with Address Detect	306
Transmitter	
Baud Rate Generator (BRG)	
Auto Baud Rate Detect	316
Baud Rate Error, Calculating	

PI	C1	6F/	LF1	825/1	829
----	-----------	-----	-----	-------	-----

Baud Rates, Asynchronous Modes	
High Baud Rate Select (BRGH Bit)	
Synchronous Master Mode	
Associated Registers	
Receive	
Transmit	
Reception	
Transmission	
Synchronous Slave Mode	
Associated Registers	
Receive	
Transmit	
Reception	
Transmission	
Extended Instruction Set	
ADDFSR 343	
E	
F	
Fail-Safe Clock Monitor69	
Fail-Safe Condition Clearing 69	
Fail-Safe Detection69	
Fail-Safe Operation 69	
Reset or Wake-up from Sleep69	
Firmware Instructions	
Fixed Voltage Reference (FVR)	
Associated Registers	
Flash Program Memory	
Erasing	
Modifying118	
Writing	
FSR Register	
FVRCON (Fixed Voltage Reference Control) Register 148	
FVRCON (Fixed Voltage Reference Control) Register 148	
1	
I I ² C Mode (MSSPx)	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	
I I ² C Mode (MSSPx) Acknowledge Sequence Timing	

BRA	344
CALL	
CALLW	
LSLF	
LSRF	347
MOVF	347
MOVIW	348
MOVLB	348
MOVWI	
OPTION	349
RESET	349
SUBWFB	351
TRIS	352
BCF	344
BSF	344
BTFSC	344
BTFSS	
CALL	
CLRF	
CLRW	
CLRWDT	
COMF	
DECF	
DECFSZ	
GOTO	
INCE	
INCESZ	
IORLW	
IORUF	
MOVWF	
NOP	
RETFIE	
RETLW	
RETURN	
RLF	
RRF	
SLEEP	
SUBLW	
SUBWF	
SWAPF	
XORLW	
XORWF	
INTCON Register	93
Internal Oscillator Block	
INTOSC	
Specifications	
Internal Sampling Switch (Rss) Impedance	
Internet Address	
Interrupt-On-Change	
Associated Registers	
Interrupts	
ADC	
Associated registers w/ Interrupts	
Configuration Word w/ Clock Sources	
Configuration Word w/ Reference Clock Sources	. 77
TMR1	
INTOSC Specifications	
IOCAF Register	
IOCAN Register	
	144
IOCAP Register	144
IOCAP Register	144 144
	144 144 146
IOCBF Register	144 144 146 145

L

LATA Register	130, 140
LATB Register	
Load Conditions	
LSLF	
LSRF	

Μ

Master Synchronous Serial Port. See MSSPx

MCLR	82
Internal	82
MDCARH Register	. 214
MDCARL Register	. 215
MDCON Register	. 212
MDSRC Register	. 213
Memory Organization	23
Data	25
Program	
Microchip Internet Web Site	.418
Migrating from other PIC Micro Devices	. 409
MOVIW	. 348
MOVLB	. 348
MOVWI	. 349
MPLAB ASM30 Assembler, Linker, Librarian	. 388
MPLAB Integrated Development Environment Software .	. 387
MPLAB PM3 Device Programmer	. 390
MPLAB REAL ICE In-Circuit Emulator System	. 389
MPLINK Object Linker/MPLIB Object Librarian	. 388
MSSPx	. 245
I ² C Mode	. 256
I ² C Mode Operation	
SPI Mode	. 248
SSPxBUF Register	. 251
SSPxSR Register	. 251

0

OPCODE Field Descriptions	
OPTION	
OPTION Register	
OSCCON Register	
Oscillator	
Associated Registers	73
Oscillator Module	
ECH	
ECL	
ECM	
HS	
INTOSC	
LP	
RC	
XT	
Oscillator Parameters	
Oscillator Specifications	
Oscillator Start-up Timer (OST)	
Specifications	
Oscillator Switching	
Fail-Safe Clock Monitor	69
Two-Speed Clock Start-up	
OSCSTAT Register	
OSCTUNE Register	
Ű	
Ρ	

P1A/P1B/P1C/P1D.See Enhanced Capture/	
Compare/PWM (ECCP)	226
Packaging	391

Marking	
PCL and PCLATH	
PCL Register	
PCLATH Register 33, 34, 35, 36, 37, 38, 39, 40,	
PCON Register	
PIE1 Register	
PIE2 Register	
PIE3 Register	
PIE4 Register	34, 97
Pinout Descriptions	
PIC16F/LF1826/27	
PIR1 Register	-
PIR2 Register	
PIR3 Register	
PIR4 Register	
PORTA	127
ANSELA Register	127
Associated Registers	132
Configuration Word w/ PORTA	132
LATA Register	35
PORTA Register	
Specifications	
PORTA Register	
PORTB	
ANSELB Register	
Associated Registers	
LATB Register	
Pin Descriptions and Diagrams	
PORTB Register	
PORTB Register	
PORTC	
ANSELC Register	138
Associated Registers	
LATC Register	
Pin Descriptions and Diagrams	
PORTC Register	
PORTC Register	
Power-Down Mode (Sleep)	
Associated Registers Power-on Reset	
Power-up Time-out Sequence	
Power-up Timer (PWRT)	
Specifications	
- 3	
PR4 Register	
PR6 Register	
Precision Internal Oscillator Parameters	
Program Memory	
Map and Stack (PIC16F/LF1826)	
Map and Stack (PIC16F/LF1826/27)	
Programming, Device Instructions	
PSTRxCON Register	
PWM (ECCP Module)	
PWM Steering	
Steering Synchronization	
PWM Mode. See Enhanced Capture/Compare/PW	
PWM Steering	
PWMxCON Register	
R	
RCREG	306
	חוור.

RCREG	306
RCREG Register	
RCSTA Register	
Reader Response	419
Read-Modify-Write Operations	

Reference Clock75
Associated Registers
Registers
ADCON0 (ADC Control 0) 158
ADCON1 (ADC Control 1) 159
ADRESH (ADC Result High) with ADFM = 0)
ADRESH (ADC Result High) with ADFM = 1)
ADRESL (ADC Result Low) with ADFM = 0)
ADRESE (ADC Result Low) with ADPM – 1)
ANSELB (PORTB Analog Select)
ANSELC (PORTC Analog Select)
APFCON0 (Alternate Pin Function Control 0) 125
APFCON1 (Alternate Pin Function Control 1)
BAUDCON (Baud Rate Control)
BORCON Brown-out Reset Control)
CCPTMRS (PWM Timer Selection Control)
CCPxCON (ECCPx Control)
CLKRCON (Reference Clock Control)
CMOUT (Comparator Output)
CMxCON0 (Cx Control) 184
CMxCON1 (Cx Control 1) 185
Configuration Word 1 52
Configuration Word 2
CPSCON0 (Capacitive Sensing Control Register 0) 333 CPSCON1 (Capacitive Sensing Control Register 1) 334
DACCON0
DACCON1
EEADRL (EEPROM Address)
EECON1 (EEPROM Control 1)
EECON2 (EEPROM Control 2) 122
EEDATH (EEPROM Data) 120
EEDATL (EEPROM Data) 120
FVRCON
INLVLA (Input Level Control PORTA)
INLVLC (Input Level Control PORTC)
INTCON (Interrupt Control)
IOCAF (Interrupt-on-Change PORTA Flag)
IOCAN (Interrupt-on-Change PORTA
Negative Edge) 144
IOCAP (Interrupt-on-Change PORTA
Positive Edge)
IOCBF (Interrupt-on-Change PORTB Flag)146 IOCBN (Interrupt-on-Change PORTB
Negative Edge)
IOCBP (Interrupt-on-Change PORTB
Positive Edge)
LATA (Data Latch PORTA)130
LATB (Data Latch PORTB) 135
LATC (Data Latch PORTC) 140
MDCARH (Modulation High Carrier
Control Register)
MDCARL (Modulation Low Carrier Control Register)215 MDCON (Modulation Control Register)
MDSRC (Modulation Source Control Register)
OPTION_REG (OPTION)
OSCCON (Oscillator Control)
OSCSTAT (Oscillator Status)72
OSCTUNE (Oscillator Tuning)73
PCON (Power Control Register)
PCON (Power Control)
PIE1 (Peripheral Interrupt Enable 1)

PIE3 (Peripheral Interrupt Enable 3)	96
PIE4 (Peripheral Interrupt Enable 4)	
PIR1 (Peripheral Interrupt Register 1)	98
PIR2 (Peripheral Interrupt Request 2)	
PIR3 (Peripheral Interrupt Request 3)	100
PIR4 (Peripheral Interrupt Request 4)	
PORTA	
PORTB	135
PORTC	140
PSTRxCON (PWM Steering Control)	244
PWMxCON (Enhanced PWM Control)	243
RCREG	316
RCSTA (Receive Status and Control)	
SPBRGH	
SPBRGL	311
Special Function, Summary	
SRCON0 (SR Latch Control 0)	173
SRCON1 (SR Latch Control 1)	
SSPxADD (MSSPx Address and Baud Rate,	
I ² C Mode)	297
SSPxCON1 (MSSPx Control 1)	294
SSPxCON2 (SSPx Control 2)	
SSPxCON3 (SSPx Control 3)	
SSPxMSK (SSPx Mask)	
SSPxSTAT (SSPx Status)	
STATUS	
T1CON (Timer1 Control)	
T1GCON (Timer1 Gate Control)	200
TRISA (Tri-State PORTA)	129
TRISB (Tri-State PORTB)	
TRISC (Tri-State PORTC)	
TXCON	205
TXSTA (Transmit Status and Control)	308
WDTCON (Watchdog Timer Control)	107
WPUA (Weak Pull-up PORTA)	131
WPUB (Weak Pull-up PORTB)	136
WPUC (Weak Pull-up PORTC)	141
RESET	
Reset	79
Reset Instruction	82
Resets	79
Associated Registers	86
Revision History	409
S	
-	
Shoot-through Current	236
Software Simulator (MPLAB SIM)	
SPBRG Register	
SPBRGH Register	
SPBRGL Register	
Special Event Trigger	
Special Function Redisters (SFRS)	33

Special Event Trigger	156
Special Function Registers (SFRs)	33
SPI Mode (MSSPx)	
Associated Registers	255
SPI Clock	251
SR Latch	171
Associated registers w/ SR Latch	175
SRCON0 Register	173
SRCON1 Register	
SSP1ADD Register	37
SSP1BUF Register	37
SSP1CON Register	
SSP1CON2 Register	37
SSP1CON3 Register	37
SSP1MSK Register	37
SSP1STAT Register	37

PIC16F/LF1825/1829

SSP2ADD Register	
SSP2BUF Register	
SSP2CON Register	
SSP2CON2 Register	
SSP2CON3 Register	
SSP2MSK Register	
SSP2STAT Register	
SSPxADD Register	
SSPxCON1 Register	
SSPxCON2 Register	
SSPxCON3 Register	
SSPxMSK Register	
SSPxOV	
SSPxOV Status Flag	
SSPxSTAT Register	
R/W Bit	
Stack	45
Accessing	45
Reset	47
Stack Overflow/Underflow	82
STATUS Register	
SUBWFB	

т

T1CON Register	33,	199
T1GCON Register		
T2CON Register		33
T4CON Register		
T6CON Register		
Temperature Indicator Module		
Thermal Considerations		366
Timer0		187
Associated Registers		189
Operation		187
Specifications		374
Timer1		191
Associated registers		201
Asynchronous Counter Mode		193
Reading and Writing		193
Clock Source Selection		192
Interrupt		195
Operation		192
Operation During Sleep		195
Oscillator		193
Prescaler		193
Specifications		374
Timer1 Gate		
Selecting Source		193
TMR1H Register		191
TMR1L Register		191
Timer2		
Associated registers		206
Timer2/4/6		203
Associated registers		206
Timers		
Timer1		
T1CON		199
T1GCON		200
Timer2/4/6		
TXCON		205
Timing Diagrams		
A/D Conversion		
A/D Conversion (Sleep Mode)		376
Acknowledge Sequence		284
Asynchronous Reception		
Asynchronous Transmission		302

Asynchronous Transmission (Back to Back)	
Auto Wake-up Bit (WUE) During Normal Operation. 318	
Auto Wake-up Bit (WUE) During Sleep 318	3
Automatic Baud Rate Calibration	3
Baud Rate Generator with Clock Arbitration	7
BRG Reset Due to SDA Arbitration During Start	
Condition	
Brown-out Reset (BOR) 372	2
Brown-out Reset Situations81	
Bus Collision During a Repeated Start Condition	
(Case 1) 289)
Bus Collision During a Repeated Start Condition	
(Case 2)	
Bus Collision During a Start Condition (SCL = 0) 288	
Bus Collision During a Stop Condition (Case 1) 290	
Bus Collision During a Stop Condition (Case 2) 290	
Bus Collision During Start Condition (SDA only) 287	
Bus Collision for Transmit and Acknowledge	
CLKOUT and I/O	
Clock Synchronization	
Clock Timing	
Comparator Output	
Enhanced Capture/Compare/PWM (ECCP)	
Fail-Safe Clock Monitor (FSCM)	
First Start Bit Timing	
Full-Bridge PWM Output	
Half-Bridge PWM Output 229, 236	5
I ² C Bus Data	2
I ² C Bus Start/Stop Bits	
I ² C Master Mode (7 or 10-Bit Transmission)	
I ² C Master Mode (7-Bit Reception)	
I ² C Stop Condition Receive or Transmit Mode	
INT Pin Interrupt	
PWM Auto-shutdown 235	5
PWM Auto-shutdown	5 1
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232	5 1 2
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233	5423
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227	5 4 2 3 7
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228	5 4 2 3 7 3
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279	5423739
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83	54237393
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83 Reset, WDT, OST and Power-up Timer 371	542373931
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83 Reset, WDT, OST and Power-up Timer 371 Send Break Character Sequence 319	5423739319
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379	54237393199
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Mode (Master Mode)251	542373931991
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83 Reset, WDT, OST and Power-up Timer 371 Send Break Character Sequence 319 SPI Master Mode (CKE = 1, SMP = 1) 379 SPI Slave Mode (CKE = 0) 380	5423739319910
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83 Reset, WDT, OST and Power-up Timer 371 Send Break Character Sequence 319 SPI Master Mode (CKE = 1, SMP = 1) 379 SPI Slave Mode (CKE = 0) 380 SPI Slave Mode (CKE = 1) 380	54237393199100
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)380Synchronous Reception (Master Mode, SREN)323	542878981991008
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)380Synchronous Reception (Master Mode, SREN)323Synchronous Transmission321	5423739319910031
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)380Synchronous Reception (Master Mode, SREN)323	54237393199100311
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)380Synchronous Reception (Master Mode, SREN)323Synchronous Transmission321Synchronous Transmission (Through TXEN)321Timer0 and Timer1 External Clock373	542373931991003113
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)380Synchronous Reception (Master Mode, SREN)323Synchronous Transmission321Synchronous Transmission (Through TXEN)321	5423739319910031135
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)380Synchronous Reception (Master Mode, SREN)323Synchronous Transmission321Synchronous Transmission (Through TXEN)321Timer0 and Timer1 External Clock373Timer1 Incrementing Edge195	54237393199100311353
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)380Synchronous Reception (Master Mode, SREN)323Synchronous Transmission321Synchronous Transmission (Through TXEN)321Timer0 and Timer1 External Clock373Timer1 Incrementing Edge195Two Speed Start-up68USART Synchronous Receive (Master/Slave)378	5 4 2 3 7 3 9 3 1 9 9 1 0 0 3 1 1 3 5 3 3
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)380Synchronous Reception (Master Mode, SREN)323Synchronous Transmission321Synchronous Transmission (Through TXEN)321Timer0 and Timer1 External Clock373Timer1 Incrementing Edge195Two Speed Start-up68	5 4 2 3 7 3 9 3 1 9 9 1 0 0 3 1 1 3 5 3 3 3 3
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)380Synchronous Reception (Master Mode, SREN)323Synchronous Transmission321Synchronous Transmission (Through TXEN)321Timer0 and Timer1 External Clock373Timer1 Incrementing Edge195Two Speed Start-up68USART Synchronous Transmission (Master/Slave)378USART Synchronous Transmission (Master/Slave)378	5 4 2 3 7 3 9 3 1 9 9 1 0 0 3 1 1 3 5 3 3 3 3
PWM Auto-shutdown235Firmware Restart234PWM Direction Change232PWM Direction Change at Near 100% Duty Cycle233PWM Output (Active-High)227PWM Output (Active-Low)228Repeat Start Condition279Reset Start-up Sequence83Reset, WDT, OST and Power-up Timer371Send Break Character Sequence319SPI Master Mode (CKE = 1, SMP = 1)379SPI Mode (Master Mode)251SPI Slave Mode (CKE = 0)380SPI Slave Mode (CKE = 1)323Synchronous Reception (Master Mode, SREN)323Synchronous Transmission321Synchronous Transmission (Through TXEN)321Timer0 and Timer1 External Clock373Timer1 Incrementing Edge196Two Speed Start-up68USART Synchronous Transmission (Master/Slave)378Wake-up from Interrupt104Timing Diagrams and SpecificationsPLL ClockPLL Clock369	5 4 2 3 7 3 9 3 1 9 9 1 0 0 3 1 1 3 5 3 3 4 9 9
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83 Reset, WDT, OST and Power-up Timer 371 Send Break Character Sequence 319 SPI Master Mode (CKE = 1, SMP = 1) 379 SPI Mode (Master Mode) 251 SPI Slave Mode (CKE = 0) 380 Synchronous Reception (Master Mode, SREN) 323 Synchronous Transmission 321 Synchronous Transmission (Through TXEN) 321 Timer0 and Timer1 External Clock 373 Timer1 Incrementing Edge 196 Two Speed Start-up 68 USART Synchronous Transmission (Master/Slave) 378 Wake-up from Interrupt 104 Timing Diagrams and Specifications PLL Clock 369 Fluing Parameter Symbology 367	5 4 2 3 7 3 9 3 1 9 9 1 0 0 3 1 1 3 5 3 3 4 9 9
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83 Reset, WDT, OST and Power-up Timer 371 Send Break Character Sequence 319 SPI Master Mode (CKE = 1, SMP = 1) 379 SPI Mode (Master Mode) 251 SPI Slave Mode (CKE = 0) 380 Synchronous Reception (Master Mode, SREN) 323 Synchronous Transmission 321 Synchronous Transmission (Through TXEN) 321 Timer0 and Timer1 External Clock 373 Timer1 Incrementing Edge 195 Two Speed Start-up 68 USART Synchronous Transmission (Master/Slave) 378 Wake-up from Interrupt 104 Timing Diagrams and Specifications 104 Timing Parameter Symbology 367	5 1
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83 Reset, WDT, OST and Power-up Timer 371 Send Break Character Sequence 319 SPI Master Mode (CKE = 1, SMP = 1) 379 SPI Mode (Master Mode) 251 SPI Slave Mode (CKE = 0) 380 Synchronous Reception (Master Mode, SREN) 323 Synchronous Transmission 321 Synchronous Transmission (Through TXEN) 321 Timer0 and Timer1 External Clock 373 Timer1 Incrementing Edge 195 Two Speed Start-up 66 USART Synchronous Transmission (Master/Slave) 378 Wake-up from Interrupt 104 Timing Diagrams and Specifications 104 Timing Parameter Symbology 367 Timing Requirements 1 ² C Bus Data 383	5 4 2 3 7 3 9 3 1 9 9 1 0 0 3 1 1 3 5 3 3 4 9 7 3 9 7 3 9 7 3 9 3 1 9 9 10 9 3 1 9 9 10 9 10 9 10 9
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83 Reset, WDT, OST and Power-up Timer 371 Send Break Character Sequence 319 SPI Master Mode (CKE = 1, SMP = 1) 379 SPI Mode (Master Mode) 251 SPI Slave Mode (CKE = 0) 380 Synchronous Reception (Master Mode, SREN) 323 Synchronous Transmission 321 Synchronous Transmission (Through TXEN) 321 Timer0 and Timer1 External Clock 373 Timer1 Incrementing Edge 195 Two Speed Start-up 68 USART Synchronous Transmission (Master/Slave) 378 Wake-up from Interrupt 104 Timing Diagrams and Specifications 104 Timing Requirements 1 ² C Bus Data 383 SPI Mode 381	5 4 2 3 7 3 1 1 1 3 5 3 3 1 1 1 3 5 3 3 1 1 1 3 5 3 3 1 1 1 3 5 3 3 1
PWM Auto-shutdown 235 Firmware Restart 234 PWM Direction Change 232 PWM Direction Change at Near 100% Duty Cycle 233 PWM Output (Active-High) 227 PWM Output (Active-Low) 228 Repeat Start Condition 279 Reset Start-up Sequence 83 Reset, WDT, OST and Power-up Timer 371 Send Break Character Sequence 319 SPI Master Mode (CKE = 1, SMP = 1) 379 SPI Mode (Master Mode) 251 SPI Slave Mode (CKE = 0) 380 Synchronous Reception (Master Mode, SREN) 323 Synchronous Transmission 321 Synchronous Transmission (Through TXEN) 321 Timer0 and Timer1 External Clock 373 Timer1 Incrementing Edge 195 Two Speed Start-up 66 USART Synchronous Transmission (Master/Slave) 378 Wake-up from Interrupt 104 Timing Diagrams and Specifications 104 Timing Parameter Symbology 367 Timing Requirements 1 ² C Bus Data 383	5 1

TMR1H Register	
TMR1L Register	
TMR2 Register	
TMR4 Register	
TMR6 Register	41
TRIS	
TRISA Register	
TRISB	
TRISB Register	
TRISC	
TRISC Register	
Two-Speed Clock Start-up Mode	67
TXCON (Timer2/4/6) Register	
TXREG	
TXREG Register	
TXSTA Register	
BRGH Bit	

U

USART

Synchronous Master Mode
Requirements, Synchronous Receive
Requirements, Synchronous Transmission 378
Timing Diagram, Synchronous Receive
Timing Diagram, Synchronous Transmission 378

۷

VREF. SEE ADC Reference Voltage

W

Wake-up on Break	
Wake-up Using Interrupts	103
Watchdog Timer (WDT)	
Modes	
Specifications	
WCOL	277, 280, 282, 284
WCOL Status Flag	277, 280, 282, 284
WDTCON Register	
WPUA Register	
WPUB Register	
WPUC Register	
Write Protection	
WWW Address	
WWW, On-Line Support	

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	PIC16F1829T ⁽²⁾ ; VDD range 1.8V to 5.5V PIC16LF1825 ⁽¹⁾ , PIC16LF1829 ⁽¹⁾ , PIC16LF1825T ⁽²⁾ , PIC16LF1829T ⁽²⁾ ; VDD range 1.8V to 3.6V	package, normal VDD limits.
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